RONETIX
DEVELOPMENT TOOLS

i.MX8MP-COMPACT-CM

CPU Module (SoM) with NXP i.MX8M-Plus

Datasheet

rev 1.0

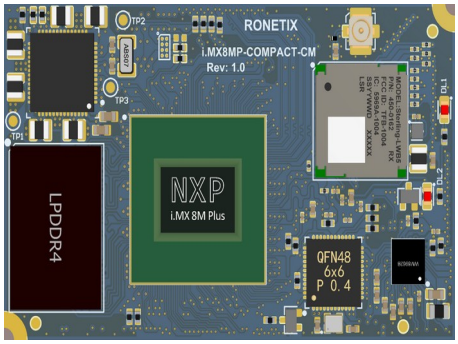

Figure 1: Top view

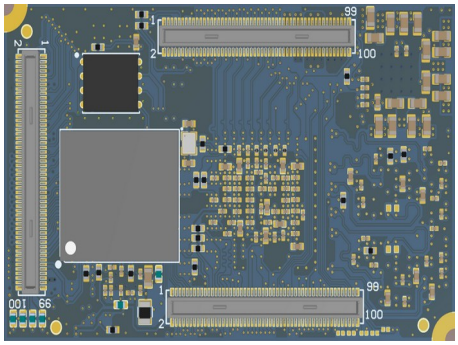

Figure 2: Bottom view

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1. Document Revision History

Revision	Date	Notes
1.0	22-March-2021	Initial release

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3. Overview

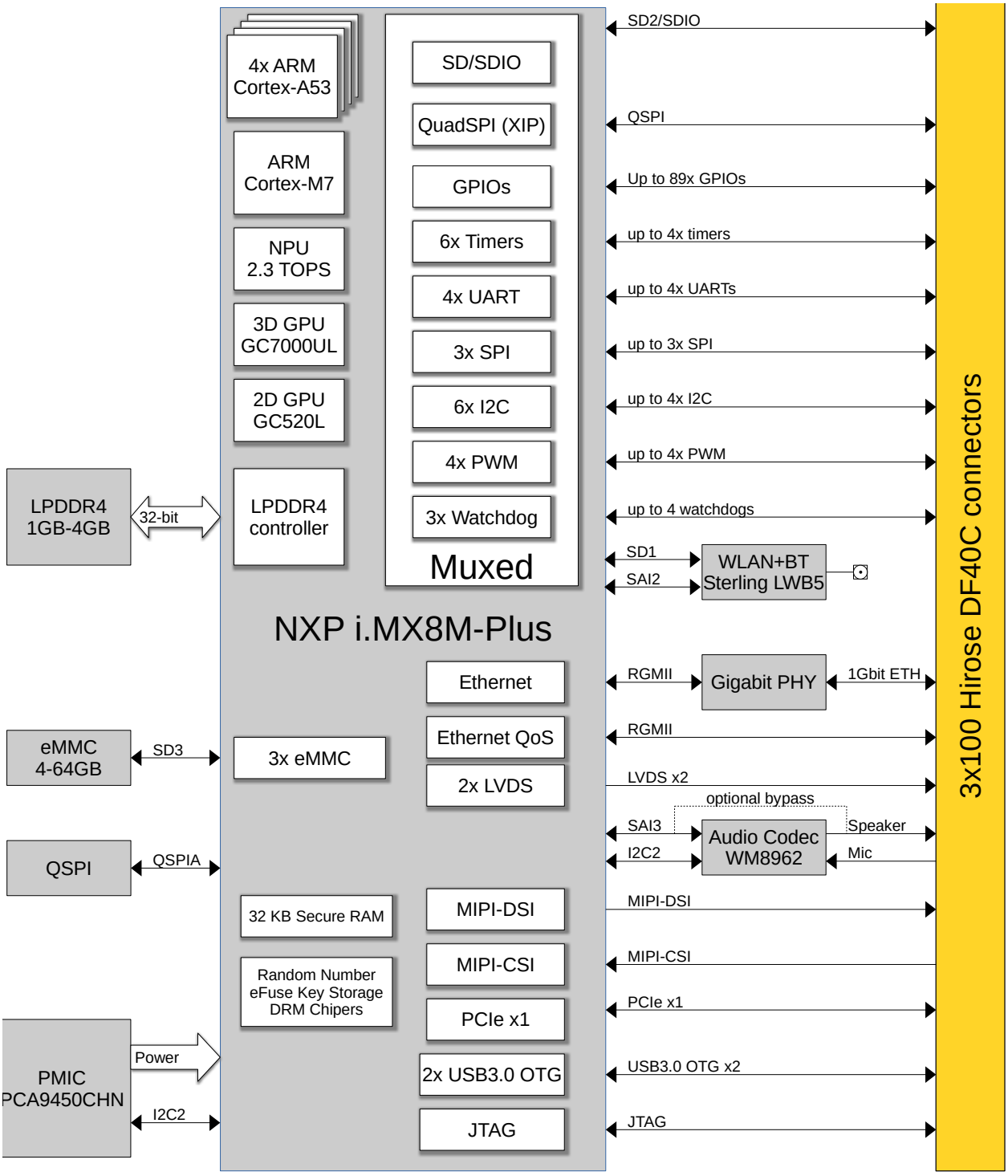
3.1 General Information

The **i.MX8MP-COMPACT-CM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX8M-Plus family focuses on neural processing unit (NPU) and vision system, advance multimedia, and industrial automation with high reliability. The i.MX8M-Plus is a powerful quad Arm® Cortex®-A53 processor with speed up to 1.8 GHz integrated with a NPU of 2.3 TOPS that greatly accelerate machine learning inference. The vision engine is composed of two camera inputs and a HDR-capable Image Signal Processor (ISP) capable of 375 Mpixels/s. The advanced multimedia capabilities include 1080p60 video encode and decode H.265 and H.264. A 3D and 2D graphic acceleration supporting 1 Gpixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces for Immersive Audio and Voice systems. For industrial applications, real time control is enabled by an integrated 800 MHz Arm® Cortex®-M7.

3.2 Highlights

CPU	• Quad ARMv8-A, 64-bit Cortex™-A53 Core, 1.8GHz • ARM® Cortex™-M7, 800MHz • Neural Processing Unit 2.3 TOPS • GPU GC7000UL with OpenCL and Vulkan support • Video Processing Unit
Memory	• RAM: 1 GiB LPDDR4 (optional: up to 4 GiB) • eMMC: 4 GiB (optional: up to 64 GiB) • QSPI NOR Flash (optional)
Display	• 2x LVDS • HDMI • MIPI DSI
Camera	• 2x MIPI-CSI, 4 data lanes
Network	• Ethernet: 10/100/1000Mbps • WiFi: Sterling LWB5, 802.11ac, dual band (optional) • Bluetooth: Bluetooth 4.2 (optional)
I/O	• PCIe 2.0, 1-lane • 2x USB3.0 OTG port • Up to 4x UART ports • MMC/SD/SDIO • Up to 3x SPI • Up to 4x I2C • Up to 4x general purpose PWM signals • GPIOs
Electrical	• Supply Voltage: 3.85 – 5.0V
Physical	• Board size: 50x30mm • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of i.MX8MP-COMPACT-CM SoM.

4.1 Power supply

i.MX8MP-COMPACT-CM uses NXP's PCA9450CHN as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M series of application processors. The PMIC regulates all power rails required on CPU module from a single 3.85V-5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU i.MX8M-PLUS

The i.MX8M-Plus Quad processors represent NXP's latest market of connected streaming audio/video devices, scanning/imaging devices, and various devices requiring high-performance, low-power processors. The i.MX8M-Plus Quad processors feature advanced implementation of a quad Arm®Cortex®-A53 core, which operates at speeds of up to 1.8 GHz integrated with a NPU of 2.3 TOPS that greatly accelerate machine learning inference. A general purpose Cortex®-M7 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3Lmemory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

4.2.1 CPU Block Diagram

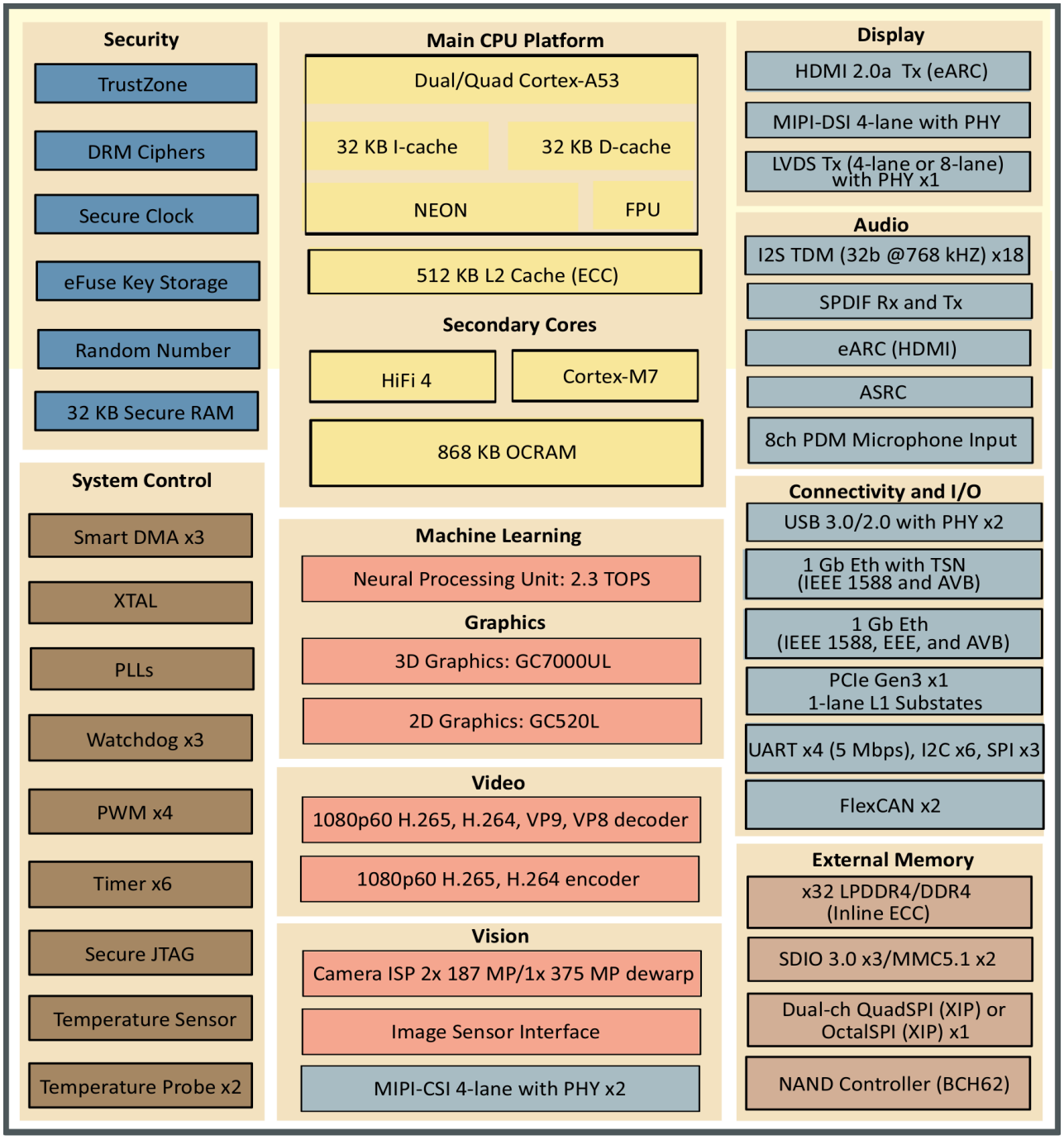


Figure 4.1: i.MX8M-Plus block diagram

4.2.2 CPU Platform

The i.MX8M-Plus processor implements up to four ARM® Cortex®-A53 cores intended for high level O/S, with an ARM® Cortex®-M7 core dedicated for real-time tasks and integrated NPU with 2.3 TOPS.

The ARM Cortex-A53 MPCore™ platform has the following features:

- Quad ARM Cortex-A53 Cores
- Target frequency of 1.8GHz
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - MPE (media processing engine) with NEON co-processor supporting SIMD architecture
- The Arm Cortex-A53 Core complex shares:
  - General interrupt controller (GIC) with 128 interrupt support
  - Global timer
  - Snoop control unit (SCU)
  - 1 MB unified I/D L2 cache
  - NEON MPE co-processor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline

The ARM Cortex-M7 platform includes the following features:

- Cortex-M4 CPU core operating at 800 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)

- 32 KByte instruction cache
- 32 KByte data cache
- 256 KByte TCM (tightly-coupled memory)

4.3 Memory

4.3.1 DRAM

i.MX8MP-COMPACT-CM is standard equipped with 1 GB LPDDR4 memory. Optionally up to 4 GB can be assembled. The data bus is 32-bit wide.

4.3.2 eMMC – non-volatile storage memory

i.MX8MP-COMPACT-CM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.4 Gigabit Ethernet

i.MX8MP-COMPACT-CM implements one full-featured 10/100/1000 Ethernet ports implemented with MAC built into the i.MX8M-Plus SoC, coupled with AR8031 RGMII Ethernet PHYs from Qualcomm. The Ethernet interface support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The i.MX8M-Plus SoC implements a second Gigabit Ethernet QoS Controller with TNS support. An external PHY is required to complete the interface to the media. The Ethernet QoS signals are available on the Hirose DF40C connectors.

4.5 WLAN

i.MX8MP-COMPACT-CM optional wireless communication is implemented with Laird Sterling LWB5 WLAN module. Sterling-LWB5 is an 802.11ac/b/g/n Dual-Band Wi-Fi+Bluetooth module based on Cypress's BCM43353 chipset. It is Dual-Band AC on 2.4GHz + 5GHz and incorporates Bluetooth 4.2. The download speed are 300Mbps on N networks and 867Mbps on AC network.

i.MX8MP-COMPACT-CM is equipped with a U.FL high frequency connector for external antenna.

4.6 Audio

i.MX8MP-COMPACT-CM implements an audio codec WM8962 (assembled optional) . The WM8962 is a low power stereo codec featuring Class D speaker drivers to provide 2W per channel into 4Ω loads. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input. Stereo 24-bit Delta Sigma converters are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface. The main clock can be input directly or generated internally by an onboard PLL, supporting most commonly used clocking schemes.

The WM8962 supports the following features:

- Stereo class D speaker driver, 2W per channel
- On-chip headphone driver 30mW output power into 16Ω
- Microphone interface
- Pop and click suppression
- DAC SNR 98 dB ('A' weighted), THD -84 dB at 48 kHz, 3.3V
- ADC SNR 94 dB ('A' weighted),THD -85 dB at 48 kHz, 3.3V
- Programmable ALC / limiter and noise gate

Please refer to the WM8960 datasheet for additional details.

4.7 LED

The i.MX8MP-COMPACT-CM features a red LED controlled by GPIO3_IO14 signal of the i.MX8M-Plus. The LED is ON when GPIO3_IO14 is logic High.

5. Hirose DF40C connectors

The i.MX8MM-COMPACT-CM exposes three 100 pin Hirose connectors DF40C-100DP-0.4V(51).

Recommended mating connector for custom board interfacing with stacking height 1.5mm is DF40C-100DS-0.4V(51). With an appropriated mated connector stacking heights from 1.5mm up to 4mm are possible.

J1	Signal iMX8MP	i.MX8MP Ball	Default	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1	GPIO2_IO07	AA29	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]
3	JTAG_TDI								
5	JTAG_TDO								
7	JTAG_TCK								
9	JTAG_TMS								
11	BOOT_MODE2								
13	BOOT_MODE1								
15	BOOT_MODE0								
17	GND								
19	SD2_nRST	AD28	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]
21	SD2_nCD	AD29	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]
23	SD2_WP	AC26	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]
25	SD2_DATA2	AA26	gpio2.IO[17]	usdhc2.DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT2	gpio2.IO[17]
27	SD2_DATA3	AA25	gpio2.IO[18]	usdhc2.DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT3	gpio2.IO[18]
29	SD2_CLK	AB29	gpio2.IO[13]	usdhc2.CLK		ECSPI2_SCLK	UART4_RX		gpio2.IO[13]
31	SD2_CMD	AB28	gpio2.IO[14]	usdhc2.CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	gpio2.IO[14]
33	SD2_DATA1	AC29	gpio2.IO[16]	usdhc2.DATA1		I2C4_SCL	UART2_TX	PDM_BIT1	gpio2.IO[16]
35	SD2_DATA0	AC28	gpio2.IO[15]	usdhc2.DATA0		I2C4_SDA	UART2_RX	PDM_BIT0	gpio2.IO[15]
37	GPIO2_IO11	W26	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]
39	GPIO4_IO22	AH16	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK		SAI2_TXD1	uart1.RX	gpio4.IO[22]
41	SAI5_RXFS	AC14	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]		I2C6_SCL		gpio3.IO[19]
43	SAI5_RXD0	AE16	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]	PWM2_OUT	I2C5_SCL	PDM_BIT0	gpio3.IO[21]
45	SAI5_MCLK	AF14	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK	PWM1_OUT	I2C5_SDA		gpio3.IO[25]
47	SAI5_RXC	AD14	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK		PDM_CLK		gpio4.IO[1]
49	SAI5_RXD1	AD16	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		PDM_BIT1		gpio4.IO[3]
51	SAI5_RXD3	AE14	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		PDM_BIT3		gpio4.IO[5]
53	SAI5_RXD2	AF16	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		PDM_BIT2		gpio4.IO[4]
55	REF_CLK_32K	A7	gpio1.IO[0]	gpio1.IO[0]					REF_CLK_32K
57	GPIO1_IO01	E8	gpio1.IO[1]	gpio1.IO[1]	PWM1_OUT				REF_CLK_24M
59	GPIO1_IO06	A3	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B
61	GPIO1_IO07	F6	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP
63	GND								
65	GPIO1_IO08	A8	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN	PWM1_OUT			usdhc2.RESET_B
67	SAI2_RXFS	AH17	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC	sai5.TX_DATA[1]	sai2.RX_DATA[1]	uart1.TX	gpio4.IO[21]
69	ENET_LED_LINK100								
71	ENET_LED_LINK1000								
73	ENET_LED_ACT								
75	CLKIN1	L24	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[2]	usdhc3.CD_B			gpio3.IO[8]
77	CLKIN2	L25	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[7]
79	GND								
81	CLKOUT1	K28							
83	CLKOUT2	L28							
85	GND								
87	SPDIF_RX	AD18	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio5.IO[4]
89	SPDIF_TX	AE18	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio5.IO[3]
91	SPDIF_EXT_CLK	AC18	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]
93	GPIO1_IO12	A5	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]
95	GPIO1_IO14	A4	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR			usdhc3.CD_B	pwm3.OUT
97	GPIO1_IO13	A6	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT
99	GPIO1_IO15	B5	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT

Figure 5.1: J1, odd pins

J1	Signal iMX8MP	i.MX8MP Ball	Default	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
2	ENET_TX1_P								
4	ENET_TX1_N								
6	ENET_RX1_P								
8	ENET_RX1_N								
10	ENET_TX2_P								
12	ENET_TX2_N								
14	ENET_RX2_P								
16	ENET_RX2_N								
18	GND								
20	SAI1_TXD6	AC12	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		ENET1_RX_ER	gpio4.IO[18]
22	SAI1_TXD7	AJ13	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK		pdm.CLK	ENET1_TX_ER	gpio4.IO[19]
24	SAI1_TXD4	AH13	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		ENET1_RGMII_TX_CTL	gpio4.IO[16]
26	SAI1_TXD5	AH14	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		ENET1_RGMII_TXC	gpio4.IO[17]
28	SAI1_TXD2	AH11	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			ENET1_RGMII_TD2	gpio4.IO[14]
30	SAI1_TXD3	AD12	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			ENET1_RGMII_TD3	gpio4.IO[15]
32	SAI1_TXD1	AJ10	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			ENET1_RGMII_TD1	gpio4.IO[13]
34	SAI1_TXD0	AJ11	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			ENET1_RGMII_TD0	gpio4.IO[12]
36	SAI1_RXD6	AH10	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.TX_SYNC	sai6.RX_SYNC		ENET1_RGMII_RD2	gpio4.IO[8]
38	SAI1_RXD7	AH12	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_SYNC	sai1.TX_DATA[4]	ENET1_RGMII_RD3	gpio4.IO[9]
40	SAI1_RXD4	AD10	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		ENET1_RGMII_RD0	gpio4.IO[6]
42	SAI1_RXD5	AE10	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.TX_DATA[0]	sai6.RX_DATA[0]	sai1.RX_SYNC	ENET1_RGMII_RD1	gpio4.IO[7]
44	SAI1_RXD2	AH9	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		PDM_BIT2	ENET1_MDC	gpio4.IO[4]
46	SAI1_RXD3	AJ8	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		PDM_BIT3	ENET1_MDIO	gpio4.IO[5]
48	SAI1_RXFS	AJ9	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC				gpio4.IO[0]
50	SAI1_RXD0	AC10	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	PDM_BIT0		gpio4.IO[2]
52	SAI1_RXD1	AF10	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		PDM_BIT1		gpio4.IO[3]
54	SAI1_RXC	AH8	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK				gpio4.IO[1]
56	SAI1_TXFS	AF12	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			ENET1_RGMII_RX_CTL	gpio4.IO[10]
58	SAI1_MCLK	AE12	gpio4.IO[20]	sai5.MCLK	SAI5_MCLK	SAI1_TXC			gpio4.IO[20]
60	SAI1_TXC	AJ12	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			ENET1_RGMII_RXC	gpio4.IO[11]
62	GND								
64	GPIO1_IO05	B4	gpio1.IO[5]	gpio1.IO[5]	m7.NMI				PMIC_READY
66	GPIO1_IO09	B8	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OU	PWM2_OUT		usdhc3.RESET_B	sdma2.EXT_EVENT[0]
68	UART1_RXD	AD6	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[22]
70	UART1_TXD	AJ3	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[23]
72	UART2_RXD	AF6	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[24]
74	UART2_TXD	AH4	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[25]
76	UART1_CTS	AE6	gpio5.IO[26]	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]
78	UART1_RTS	AJ4	gpio5.IO[27]	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]
80	UART4_RXD	AJ5	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]
82	UART4_TXD	AH5	gpio5.IO[29]	uart4.TX	uart2.RTS_B				gpio5.IO[29]
84	I2C4_SDA	AD8	gpio5.IO[21]	i2c4.SDA	pwm1.OUT				gpio5.IO[21]
86	I2C4_SCL	AF8	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]
88	GND								
90	SAI3_RXFS	AJ19	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC	sai3.RX_DATA[1]	SPDIF1_IN	gpio4.IO[28]
92	SAI3_RXD	AF18	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]		uart2.RTS_B	gpio4.IO[30]
94	SAI3_TXC	AH19	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]		uart2.TX	gpio5.IO[0]
96	SAI3_TXD	AH18	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]
98	SAI3_MCLK	AJ20	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]
100	SAI3_TXFS	AC16	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CLK	sai5.RX_DATA[1]	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]

Figure 5.2: J1, even pins

J2	Signal iMX8MP	i.MX8MP Ball		Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1									
3	USB2_VBUS	D12							
5									
7	USB1_VBUS	A11							
9	GND								
11	LVDS0_CLK_N	G28							
13	LVDS0_CLK_P	F29							
15	GND								
17	LVDS0_TX3_N	J28							
19	LVDS0_TX3_P	H29							
21	GND								
23	LVDS0_TX2_N	H28							
25	LVDS0_TX2_P	G29							
27	GND								
29	LVDS0_TX1_N	F28							
31	LVDS0_TX1_P	E29							
33	GND								
35	LVDS0_TX0_N	E28							
37	LVDS0_TX0_P	D29							
39	GND								
41	MX8_ONOFF	G22							
43	I2C1_SCL	AC8	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[14]
45	I2C1_SDA	AH7	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[15]
47	POR_B	J29							
49	I2C3_SCL	AJ7	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]
51	I2C3_SDA	AJ6	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]
53	ECSPI2_MISO	AH20	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]
55	ECSPI2_MOSI	AJ21	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[11]
57	ECSPI1_MISO	AD20	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]
59	ECSPI1_MOSI	AC20	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[7]
61	ECSPI1_SS0	AE20	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]
63	ECSPI2_SS0	AJ22	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]
65	VDD_1V8								
67	VDD_1V8								
69	VDD_1V8								
71	VDD_3V3								
73	VDD_3V3								
75	VDD_3V3								
77	VSYS								
79	VSYS								
81	VSYS								
83	VSYS								
85	VSYS								
87	VSYS								
89	GND								
91	GND								
93	GND								
95	GND								
97	GND								
99	GND								

Figure 5.3: J2, odd pins

J2	Signal iMX8MP	i.MX8MP Ball		Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
2	USB2_D_P	D14							
4	USB2_D_N	E14							
6	USB1_D_P	D10							
8	USB1_D_N	E10							
10	GND								
12	PCIE_REF_CLK_P	D16							
14	PCIE_REF_CLK_N	E16							
16	GND								
18	PCIE_TX_P	A15							
20	PCIE_TX_N	B15							
22	GND								
24	PCIE_RX_P	A14							
26	PCIE_RX_N	B14							
28	GND								
30	CSI1_D3_P	D26							
32	CSI1_D3_N	E26							
34	GND								
36	CSI1_D2_P	D24							
38	CSI1_D2_N	E24							
40	GND								
42	CSI1_CLK_P	D22							
44	CSI1_CLK_N	E22							
46	GND								
48	CSI1_D1_P	D20							
50	CSI1_D1_N	E20							
52	GND								
54	CSI1_D0_P	D18							
56	CSI1_D0_N	E18							
58	GND								
60	SYS_nRST	PMIC							
62	ECSPI1_SCLK	AF20	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[6]
64	ECSPI2_SCLK	AH21	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[10]
66	VDD_1V8								
68	VDD_1V8								
70	VDD_1V8								
72	VDD_3V3								
74	VDD_3V3								
76	VDD_3V3								
78	VSYS								
80	VSYS								
82	VSYS								
84	VSYS								
86	VSYS								
88	VSYS								
90	GND								
92	GND								
94	GND								
96	GND								
98	GND								
100	GND								

Figure 5.4: J2, even pins

J3	Signal iMX8MP	i.MX8MP Ball		Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
1	DSI_D0_P	A16							
3	DSI_D0_N	B16							
5	GND								
7	DSI_D1_P	A17							
9	DSI_D1_N	B17							
11	GND								
13	DSI_CLK_P	A18							
15	DSI_CLK_N	B18							
17	GND								
19	DSI_D2_P	A19							
21	DSI_D2_N	B19							
23	GND								
25	DSI_D3_P	A20							
27	DSI_D3_N	B20							
29	GND								
31	LVDS1_TX0_P	A26							
33	LVDS1_TX0_N	B26							
35	GND								
37	LVDS1_TX1_P	A27							
39	LVDS1_TX1_N	B27							
41	GND								
43	LVDS1_CLK_P	A28							
45	LVDS1_CLK_N	B28							
47	GND								
49	LVDS1_TX2_P	B29							
51	LVDS1_TX2_N	C28							
53	GND								
55	LVDS1_TX3_P	C29							
57	LVDS1_TX3_N	D28							
59	GND								
61	SAI3_RXC	AJ19							gpio4.IO[29]
63	HDMI_DDC_SDA	AF22							
65	HDMI_DDC_SCL	AC22							
67	HDMI_CEC	AD22							
69	HDMI_HPD	AE22							
71	BT_REG_ON	U26							gpio2.IO[6]
73	WL_REG_ON	W25		SD1_RESET_B	ENET1_TX_CLK_IN		I2C3_SCL	UART3_RTS_B	gpio2.IO[10]
75	GPIO2_IO09	U25							
77	GPIO2_IO08	AA28							
79	SAI2_TXFS	AJ17			SAI5_TXD1		SAI2_TXD1	UART1_CTS_B	gpio4.IO[24]
81	SAI2_TXD	AH16			SAI5_TXD3		FLEXCAN2_TX		gpio4.IO[26]
83	SAI2_RXD	AF18			SAI5_TXD0		SAI2_TXD1	UART1_RTS_B	gpio4.IO[23]
85	SAI2_TXC	AH15			SAI5_TXD2		FLEXCAN1_RX		gpio4.IO[25]
87	SAI2_MCLK	AJ15			SAI5_MCLK		FLEXCAN2_RX		gpio4.IO[27]
89	GND								
91	I2C2_SCL	AH6				SD3_CD_B	ECSPI1_MISO		gpio5.IO[16]
93	I2C2_SDA	AE8				SD3_WP	ECSPI1_SS0		gpio5.IO[17]
95	DMIC_CLK	WM8962B							
97	VSD_3V3								
99	VSD_3V3								

Figure 5.5: J2, odd pins

J3	Signal iMX8MP	i.MX8MP Ball		Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5
2	CSI2_D3_P	A21							
4	CSI2_D3_N	B21							
6	GND								
8	CSI2_D2_P	A22							
10	CSI2_D2_N	B22							
12	GND								
14	CSI2_CLK_P	A23							
16	CSI2_CLK_N	B23							
18	GND								
20	CSI2_D1_P	A24							
22	CSI2_D1_N	B24							
24	GND								
26	CSI2_D0_P	A25							
28	CSI2_D0_N	B25							
30	GND								
32	USB2_TX_P	A13							
34	USB2_TX_N	B13							
36	GND								
38	USB2_RX_P	A12							
40	USB2_RX_N	B12							
42	GND								
44	USB1_TX_P	A10							
46	USB1_TX_N	B10							
48	GND								
50	USB1_RX_P	A9							
52	USB1_RX_N	B9							
54	GND								
56	HDMI_EARC_P	AJ23							
58	HDMI_EARC_N	AH22							
60	GND								
62	HDMI_TX2_P	AH27							
64	HDMI_TX2_N	AJ27							
66	GND								
68	HDMI_TX1_P	AH26							
70	HDMI_TX1_N	AJ26							
72	GND								
74	HDMI_TX0_P	AH25							
76	HDMI_TX0_N	AJ25							
78	GND								
80	HDMI_CLK_P	AH24							
82	HDMI_CLK_N	AJ24							
84	GND								
86	MIC	WM8962B							
88	DMIC_DAT	WM8962B							
90	HEADPHONE_L	WM8962B							
92	HEADPHONE_R	WM8962B							
94	SPK_RN	WM8962B							
96	SPK_RP	WM8962B							
98	SPK_LN	WM8962B							
100	SPK_LP	WM8962B							

Figure 5.6: J3, even pins

6. CPU Module interfaces

6.1 Display interfaces

i.MX8MP-COMPACT-CM provides the following display interfaces:

- MIPI DSI

  The MIPI-DSI interface is based on the four-lane MIPI display interface available with the iMX8M-Plus SoC. The DSI signals are available on the HIROSE DF40C connectors.

  The following main features are supported:

- Up to 4 data lanes support D-PHY
- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Maximum resolution ranges up to FHD (1920 x 1440 @ 60 Hz)
- Supports High Speed and Low Power operation
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

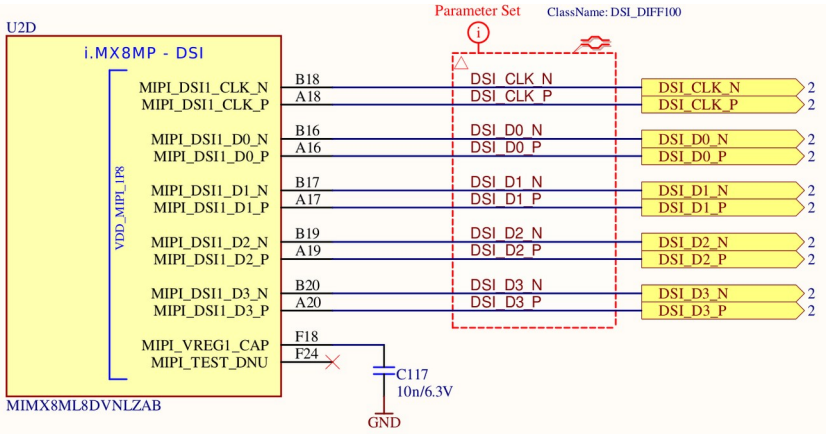


Figure 6.1: MIPI-DSI

- The i.MX8M-Plus SoC implements a LVDS Display Bridge used to connect the LCDIF to External LVDS Display Interface. LDB supports two channels, each channel has following signals:
  - One clock pair
  - Four data pairs
  - Each signal pair contains LVDS special differential pad (PadP, PadM).

  Both LVDS channels are available on the Hirose DF40C connectors.

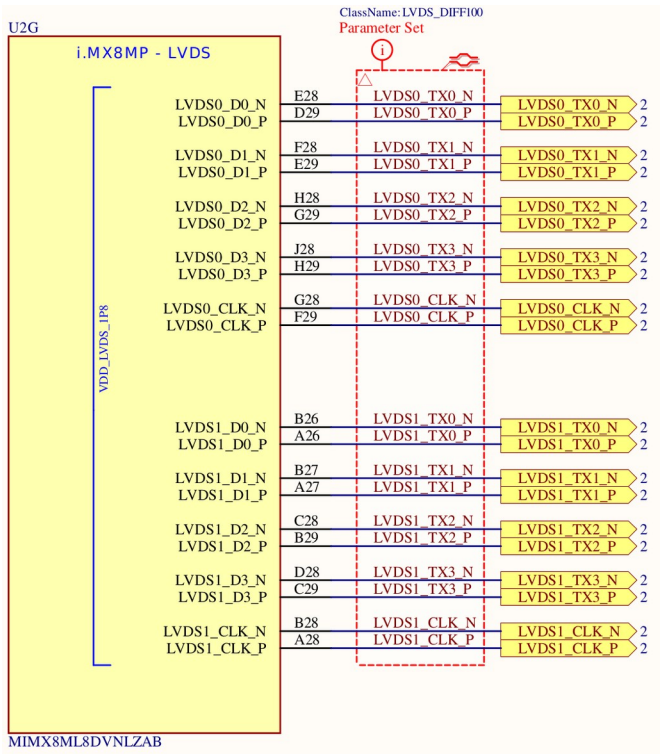


Figure 6.2: LVDS Interface

6.2 MIPI-CSI Camera interface

i.MX8MP-COMPACT-CM MIPI-CSI interface is derived from the four-lane MIPI-CSI host controller (MIPI_CSI) integrated into the iMX8M-Plus SoC. The CSI2 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between i.MX8MP-COMPACT-CM and a MIPI CSI-2 compliant camera sensor. The following main features are supported:

- Support primary and secondary Image format
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Support up to 4 lanes of D-PHY
- Interfaces
  - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification

- AMBA3.0 APB Slave for Register configuration.
- Image output data buswidth : 32 bits
- Supports data interleave

- Image memory
  - Size of SRAM is 4KB
- Pixel clock can be gated when no ppi data is coming.

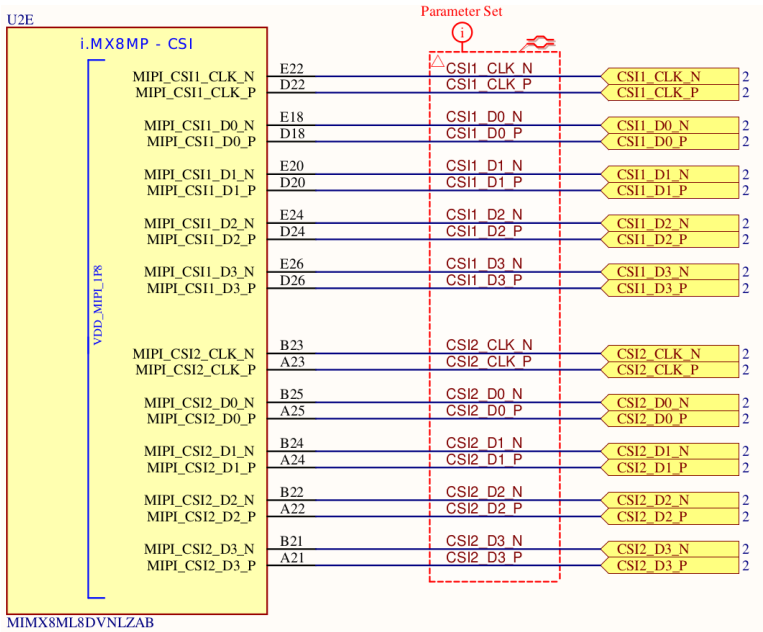


Figure 6.3: MIPI-CSI

6.3 USB interface

The i.MX8M-Plus SoC is equipped with two USB OTG controllers and PHYs. Each USB instance contains a USB 3.0 core. Both ports support dual-role functionality. The USB ports support the following main features:

- Complies with USB specification rev 3.0 (xHCI compatible)
- Supports operation as a standalone USB host controller
- USB dual-role operation and can be configured as host or device
- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low speed (1.5 Mbit/s) operations.
- Supports operation as a standalone single port USB

- Supports four programmable, bidirectional USB endpoints
- Supports system memory interface with 40-bit addressing capability

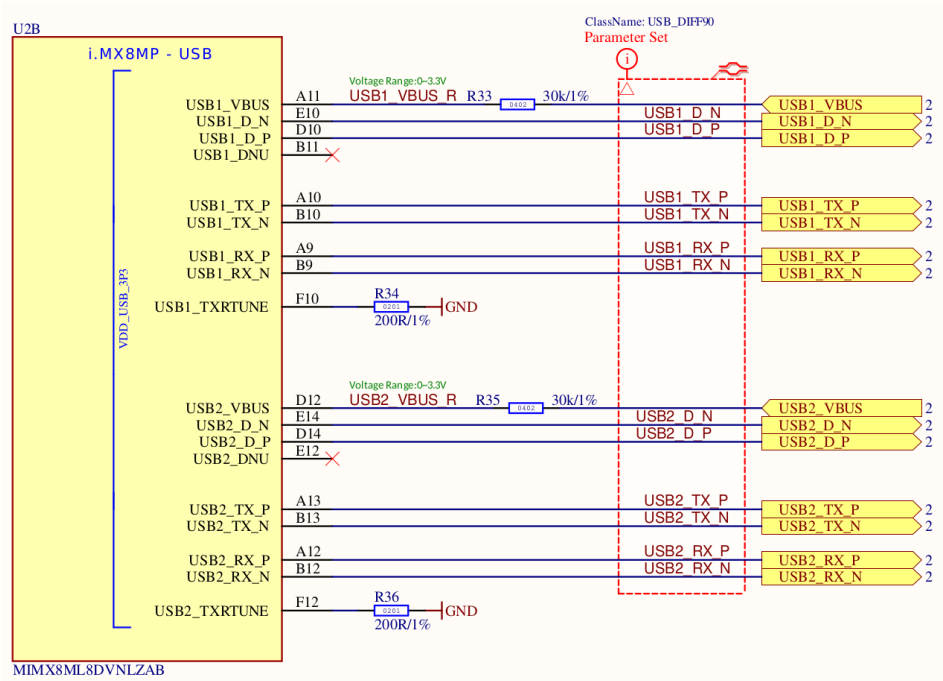


Figure 6.4: USB

6.4 PCI-Express

The i.MX8M-Plus SoC is equipped with one single lane PCI Express port (PCIe) Revision 4.0, Version 0.7. The PCI Express ports support the following main features:

- Supports Root Complex (RC) and Endpoint (EP) configurations
- Maximum link speed up to Gen3 (8 GT/s)
- x1 link width
- 128-byte maximum payload size (MAX_PAYLOAD_SIZE)
- 32- and 64-bit PCI Express address support
- Supports accesses to all PCI Express memory and I/O address spaces (RC mode requestor only)
- Supports posting of processor-to-PCI Express and PCI Express-to-memory writes
- Embedded DMA

- AXI3 bridge
- Credit-based flow control management handled by PCI Express core
- One Virtual Channel (VC0)
- PCI Express configuration space registers with Type 0 Header in EP mode and Type 1 Header in RC mode
- Internal Address Translation Unit
- Resizable BAR (RBAR) with Expanded RBAR support
- Configurable BAR Filtering, I/O Filtering, Configuration Filtering and Completion Lookup/Timeout
- Supports Completion Timeout Ranges
- Extended Tag Support
- Supports strong and relaxed transaction ordering rules
- Configurable Filtering Rules for Posted, Non-posted, and Completion Traffic
- ECRC Generation and Checking
- Baseline and Advanced Error Reporting (AER) support
- PCI Express Advanced Error Reporting (AER) with Multiple Header Logging
- Supports PCI Express messages and interrupts
- Supports 64-bit MSI interrupts
- Internal MSI-X Generation Module
- MSI and MSI-X with Per-Vector Masking (PVM), Extended message data for MSI
- Latency Tolerance Reporting (LTR)
- ID-Based Ordering (IDO)
- PASID
- L1 Substates (L1SS)
- Separate Refclk with Independent Spread Spectrum Clocking (SRIS)
- Lightweight Notifications (LN)
- Readiness Notifications (RN)
- PCI Express Active State Power Management (ASPM)

- Vital Product Data (VPD)
- Power Gating (UPF) Support
- Advanced Power and Clock Management

The PCIe controller implementation is compatible with the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

On i.MX8MP-COMPACT-CM SoM PCIe is connected to the Hirose DF40C connector and requires an external 100MHz PCIe compliant reference clock.

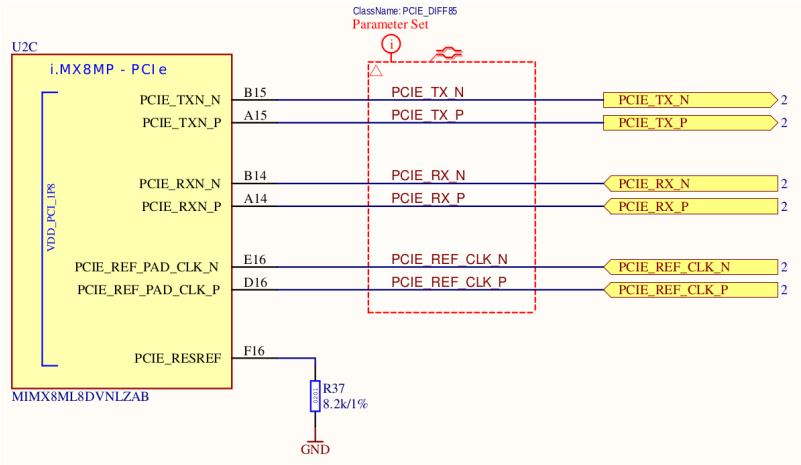


Figure 6.5: PCIe

6.5 MMC, SD, SDIO

The i.MX8M-Plus SoC is equipped with three MMC/SD/SDIO controller IPs (uSDHC). On i.MX8MP-COMPACT-CM SD3 is connected to the eMMC, SD1 is connected to the WiFi module, SD2 is available on the Hirose DF40C connector.

The uSDHC supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.1/v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.

- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- Card bus clock frequency up to 208 MHz
- Supports 1-bit/4-bit SD and SDIO modes, and 1-bit/4-bit/8-bit MMC modes
  - Up to 832 Mbps of data transfer for SDIO cards using four parallel data lines in the Single Data Rate (SDR) mode
  - Up to 400 Mbps of data transfer for SDIO card using four parallel data lines in the Dual Data Rate (DDR) mode
  - Up to 832 Mbps of data transfer for SDXC cards using four parallel data lines in the Single Data Rate (SDR) mode
  - Up to 400 Mbps of data transfer for SDXC card using four parallel data lines in the Dual Data Rate (DDR) mode
  - Up to 1600 Mbps of data transfer for MMC cards using eight parallel data lines in the Single Data Rate (SDR) mode
  - Up to 3200 Mbps of data transfer for MMC cards using eight parallel data lines in the Dual Data Rate (DDR) mode
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes; also supports interrupt period
- Embodies two fully configurable 256x32-bit FIFO for read/write data
- Supports internal and external DMA capabilities
- Support voltage selection by configuring vendor-specific register bit
- Supports Advanced DMA to perform linked memory access

- support Command queue mechanism

6.6 UART

The i.MX8MP-COMPACT-CM exposes up to 4 UART interfaces some of which are multiplexed with other peripherals.

The i.MX8M-Plus UART supports the following features:

- High-speed TIA/EIA-232-F compatible
- 9-bit or Multidrop mode (RS-485) support
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

6.7 I2C

The i.MX8M-Plus SoC is equipped with four I2C bus interfaces. I2C1, I2C2, I2C3 and I2C4 are available on the Hirose DF40C connector. I2C2 is used internally and it is also available on Hirose DF40C. The following general features are supported by all I2C bus interfaces:

- Compliant with I2C specification
- Multimaster operation
- Software programmability for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer

- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated Start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V	i.MX8MM-COMPACT-MB: Camera on CSI1, 3.3V*	(0x3C<<1)+RW
	i.MX8MM-COMPACT-MB: USB3.0 Power Switch, 3.3V*	(0x050<<1)+RW
	i.MX8MM-COMPACT-MB: RTC clock, 3.3V*	(0x51<<1)+RW
	i.MX8MM-COMPACT-MB: miniPCIEe Ref. Clock, 3.3V*	(0x6A<<1)+RW
	i.MX8MM-COMPACT-MB: Audio Codec, 3.3V*	(0x1A<<1)+RW
I2C2 1.8V	i.MX8MP-COMPACT-CM: PMIC control	(0x25<<1)+RW
	i.MX8MP-COMPACT-CM: Audio Codec	(0x1A<<1)+RW
I2C3 1.8V	i.MX8MM-COMPACT-MB: PCIe M.2, 3.3V*	
	i.MX8MM-COMPACT-MB: Camera on CSI2, 3.3V*	(0x3C<<1)+RW

Note: 3.3V* - through voltage translator

Figure 6.6: I2C address usage

6.8 SPI

Up-to three SPI interfaces are accessible through the i.MX8MP-COMPACT-CM base board interface. The SPI interfaces are derived from i.MX8M-Plus integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.

- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

6.9 PWM

Up to four PWM output signals are available at the i.MX8MP-COMPACT-CM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

6.10 GPIO

Up-to 96 of the i.MX8M-Plus general purpose input/output (GPIO) signals are available on the Hirose DF40C connector. When configured as an output, it is possible to write to an i.MX8M-Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M-Plus register. In addition GPIOs peripheral can produce interrupts.

6.11 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the Hirose DF40C connector.

7. Power Supply

7.1 Power supply from base board

i.MX8MP-COMPACT-CM is powered by regulated DC supply 3.85-5.0V

Signal	Type	Description
VIN_4V2	Power input	Main Power Supply 3.85-5.0V
GND	Power input	Common ground

7.2 Power supply provided to base board

i.MX8MP-COMPACT-CM provides 1.8V and 3.3V power supplies to the Hirose DF40C connector.

Signal	Type	Description
VDD_1V8	Power output	1.8V, Max. 0.5A
VDD_3V3	Power output	3.3V, Max. 1.5A

7.3 System Signals

Signal	Type	Description
MX8_ONOFF	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_nRST	Input	PMIC Power On signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	MIn	Max	Unit
VIN_4V2 – Main Power Supply	-0.3	5.25	V
USB_VBUS - USB_HOST_VBUS, USB_OTG_VBUS	-0.3	5.25	V

8.2 Recommended Operating Conditions

Parameter	MIn	Typ	Max	Unit
VIN_4V2 – Main Power Supply	3.8	4.2	5.0	V
VIN_4V2 – recommended source capability		4.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Cooling

A cooling solution should be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the iMX8MM-COMPACT-CM temperature specifications.

11. Mechanical Drawings

All dimensions are in millimeters.

The height of all parts is < 2mm.

The base board connector provides 1.5mm board to board clearance.

Board thickness is 1.0mm

11.1 Base board mounting

i.MX8MP-COMPACT-CM SoM has two mounting quarter-holes for mounting to the base board which are plated and connected to GND.

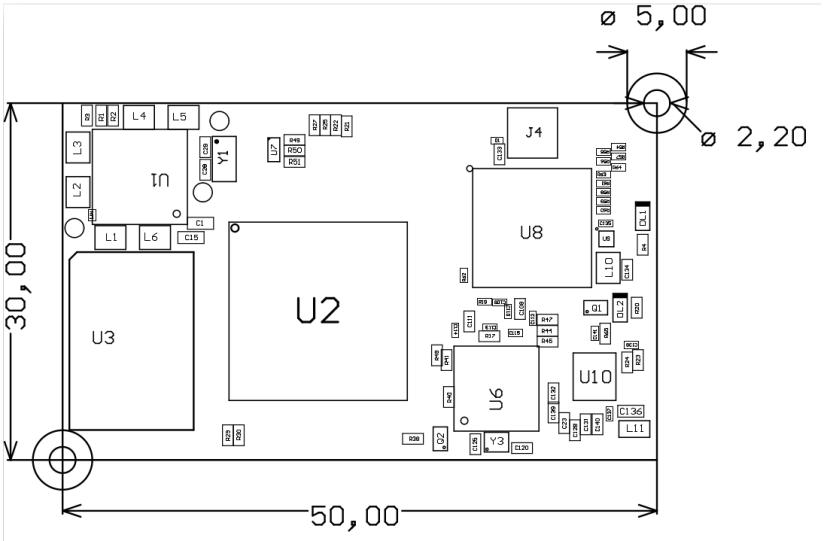


Figure 11.1: Assembly drawing

11.2 Standoffs

Fix i.MX8MP-COMACT-CM to the base board by mounting two spacers with suitable screws. The spacers should be:

- M2x0.4, length 1.5mm

12. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

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