COVER PAGE

i.MX8M-CM
Variant: Full

21.09.2021

SVN Revision: 1482 [Locally Modified]

SEQ One step 2mS	PWR	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS	3	3.3	3.6	2
2	VDD_SNVS	0.81	0.9	0.99	2
RTC_RESET_B					
3	VDD_SOC/VDDA_0P9	0.81	0.9	0.99	3600
4	VDD_GPU	0.81	0.9/1.0	1.1	2000
4	VDD_VPU	0.81	0.9/1.0	1.1	1000
4	VDD_DRAM	0.81	1.0	1.05	2500
4	VDD_ARM	0.81	0.9/1.0	1.1	4000
5	VDDA_1P8_xxx	1.62	1.8	1.89	250
5	VDDA_DRAM	1.71	1.8	1.89	50
6	NVCC_DRAM		1.1/1.2/1.35		2170
6	NVCC_3V3	3	3.3	3.6	100
6	NVCC_1V8	1.65	1.8	1.95	450
7	3.3V PHY	3.069	3.3	3.63	100
7	1.8V PHY	1.674	1.8	1.98	50
7	0.9V PHY	0.837	0.9	0.99	250
POR_B					

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

I2C USAGE AND ADDRESS TABLE

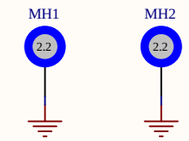
NAME	PERIPHERAL	ADDRESS
I2C1	*i.MX8-MB: USB3.0 Power Switch*	*(0x050<<1)+RW*
	i.MX8-MB: RTC clock	*(0x051<<1)+RW*
	i.MX8-MB: miniPCIEe Ref. Clock	*(0x6A<<1)+RW*
	i.MX8-MB: Camera on CSI1	*(0x3C<<1)+RW*
I2C2 only on CM	*i.MX8-CM: PMIC control*	*(0x4B<<1)+RW*
	i.MX8-CM: WiFi Ref. Clock	*(0x68<<1)+RW*
	i.MX8-CM: EEPROM	*(0x50<<1)+RW*
	i.MX8-CM: Audio Codec	*(0x1A<<1)+RW*
	i.MX8-CM: LVDS	*(0x2C<<1)+RW*
I2C3	*i.MX8-MB: mPCIe connector*	
	i.MX8-MB: Camera on CSI2	*(0x3C<<1)+RW*

PCB1

PCB
Printed circuits board

PCB_iMX8M-CM

Mounting Holes



Mounting holes 5mm pad 2.2mm drill
BOARD MOUNTING HOLES - ONE IN EACH CORNER

Fiducials

FIDICIALS 3x TOP

FIDICIALS 3x BOTTOM

Title: COVER PAGE			Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
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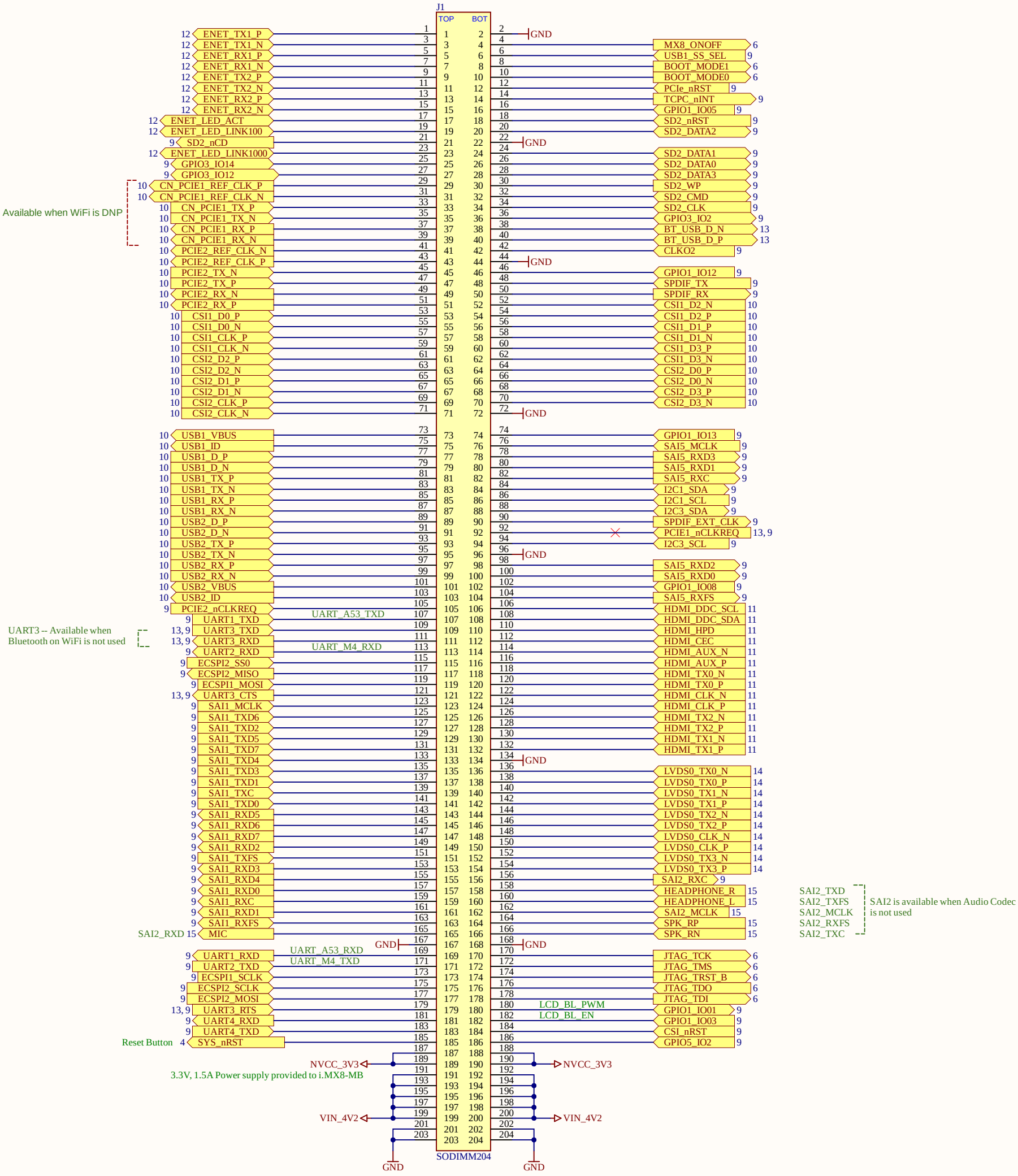
File: 01_Title_Page.SchDoc			

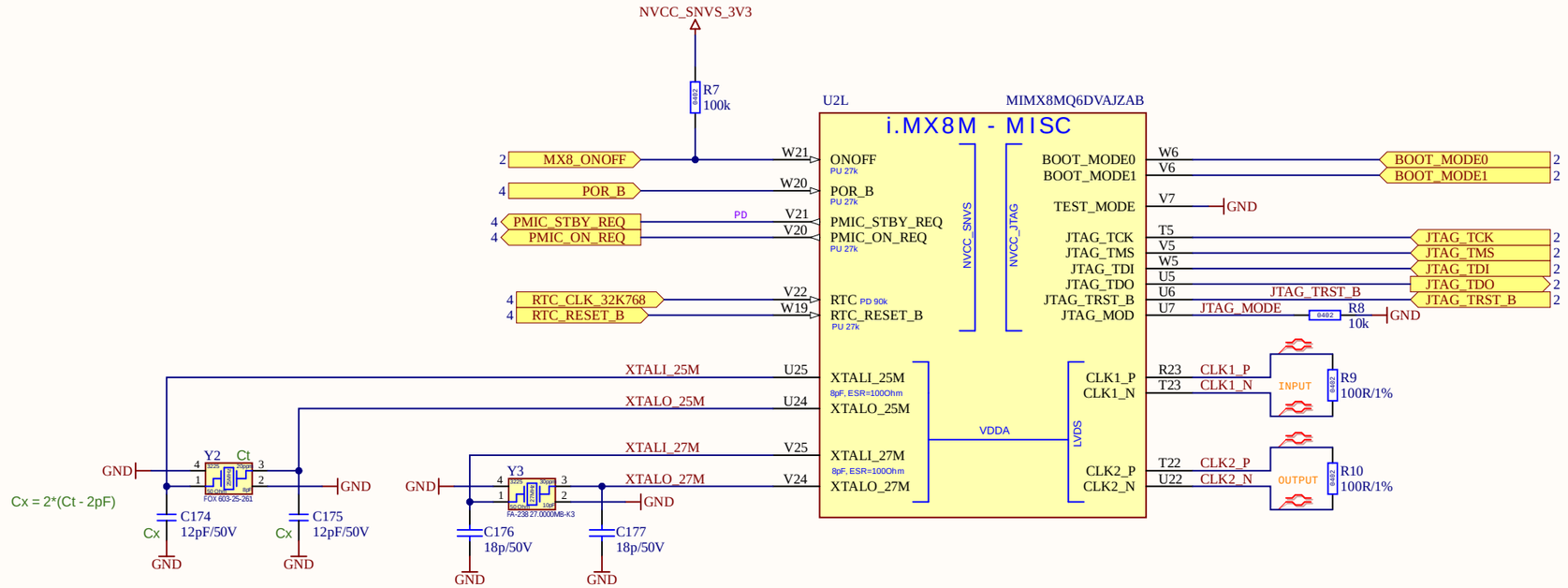
SODIMM204



Title	***SODIMM204***		*Ronetix GmbH*
Size: A3	Number: 2	Revision: 2.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 15:44:28	Sheet 2 of 16	*1220 Vienna*
File: 02_SODIMM204.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

CPU Clocks, RESET



DESIGN NOTE:
i.MX8-CM requires 3 crystal oscillators for 25MHz: CPU, ETH, WiFi.
It is as good idea to use only one high precision crystal (FOX 603-25-261) connected to the CPU. Other modules will receive 25MHz clock from CLKO_25MHz, CPU ball K7.
Note: The CPU should be configured to provide 25MHz clock on ball K7 (GPIO1_IO14).

Title: *CPU Clocks, RESET*			*Ronetix GmbH*
Size: A3	Number: 6	Revision: 2.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 15:44:28	Sheet 6 of 16	*1220 Vienna*
File: 06_CPU_CLK_RST.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

eMMC, QSPI, I2C EEPROM

eMMC

Max 80mA@3.3V
NVCC_3V3

Max 180mA@1.8V
VDD_1V8

R38 4k7
R39 4k7
R40 4k7

C212 4u7/6.3V
C213 100n/6.3V
C214 100n/6.3V

MTFC16GAKAECN-2M WT
MT53B1024M32D4NQ-062
MT25QL256ABA1EW9-0SIT
4GB KLM4G1FEPD-B031
8GB KLM8G1GEME-B041

U12A KLM4G1FETE-B041

eMMC - 4GB
BGA153, 11x10mm

SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
SD1_DATA4
SD1_DATA5
SD1_DATA6
SD1_DATA7
SD1_CMD
SD1_CLK
SD1_nRST

DAT0 A3
DAT1 A4
DAT2 A5
DAT3 B2
DAT4 B3
DAT5 B4
DAT6 B5
DAT7 B6
CMD M5
CLK M6
RST K5

VCC1 E6
VCC2 F5
VCC3 J10
VCC4 K9

VCCQ1 C6
VCCQ2 M4
VCCQ3 N4
VCCQ4 P3
VCCQ5 P5

VDD_1V8

C216 100n/6.3V
C217 100n/6.3V
C218 100n/6.3V
C215 4u7/6.3V

VDDIM C2
eMMC_VDDIM

C219 100n/6.3V
C220 100n/6.3V

VSSQ1 C4
VSSQ2 N2
VSSQ3 N5
VSSQ4 P4
VSSQ5 P6

DS H5
SD1_STROBE

VSS1 A6
VSS2 E7
VSS3 G5
VSS4 H10
VSS5 J5
VSS6 K8

GND

eMMC 5.0 Footprint

U12B KLM4G1FETE-B041

RFU1 A7
RFU2 E5
RFU3 E8
RFU4 E9
RFU5 E10
RFU6 F10
RFU7 G10
RFU8 K6
RFU9 K7
RFU10 K10
RFU11 P10

NC_P14 P14
NC_P13 P13
NC_P12 P12
NC_P11 P11
NC_P9 P9
NC_P8 P8
NC_P7 P7
NC_P2 P2
NC_P1 P1

NC_A1 A1
NC_A2 A2
NC_A8 A8
NC_A9 A9
NC_A10 A10
NC_A11 A11
NC_A12 A12
NC_A13 A13
NC_A14 A14
NC_B1 B1
NC_B7 B7
NC_B8 B8
NC_B9 B9
NC_B10 B10
NC_B11 B11
NC_B12 B12
NC_B13 B13
NC_B14 B14
NC_C1 C1
NC_C3 C3
NC_C5 C5
NC_C7 C7
NC_C8 C8
NC_C9 C9
NC_C10 C10
NC_C11 C11
NC_C12 C12
NC_C13 C13
NC_C14 C14
NC_D1 D1
NC_D2 D2
NC_D3 D3
NC_D4 D4
NC_D12 D12
NC_D13 D13
NC_D14 D14

NC_N14 N14
NC_N13 N13
NC_N12 N12
NC_N11 N11
NC_N10 N10
NC_N9 N9
NC_N8 N8
NC_N7 N7
NC_N6 N6
NC_N3 N3
NC_N1 N1
NC_M14 M14
NC_M13 M13
NC_M12 M12
NC_M11 M11
NC_M10 M10
NC_M9 M9
NC_M8 M8
NC_M7 M7
NC_M3 M3
NC_M2 M2
NC_M1 M1
NC_L14 L14
NC_L13 L13
NC_L12 L12
NC_L3 L3
NC_L2 L2
NC_L1 L1
NC_K14 K14
NC_K13 K13
NC_K12 K12
NC_K3 K3
NC_K2 K2
NC_K1 K1

NC_E1 E1
NC_E2 E2
NC_E3 E3
NC_E12 E12
NC_E13 E13
NC_E14 E14
NC_F1 F1
NC_F2 F2
NC_F3 F3
NC_F12 F12
NC_F13 F13
NC_F14 F14
NC_G1 G1
NC_G2 G2
NC_G3 G3
NC_G12 G12
NC_G13 G13
NC_G14 G14
NC_H1 H1
NC_H2 H2
NC_H3 H3
NC_H12 H12
NC_H13 H13
NC_H14 H14
NC_J1 J1
NC_J2 J2
NC_J3 J3
NC_J12 J12
NC_J13 J13
NC_J14 J14

QSPI NOR FLASH - 512 MBIT

NVCC_3V3

R16 10k

U3 30mA max

QSPIA_DATA0 SI/SIO0
QSPIA_DATA1 SO/SIO1
QSPIA_DATA2 WP/SIO2
QSPIA_DATA3 HOLD/SIO3
QSPIA_nSS0 CS
QSPIA_SCLK SCLK

VCC 3.3V
GND
EPAD

C37 4u7/6.3V
C38 100n/6.3V

MX25L51245GZ2I-08G
8-WSON

I2C EEPROM - 512 KBIT

Board ID

DESIGN NOTE:
I2C address: (0x50<<1)+RW

C221 100n/6.3V

U13

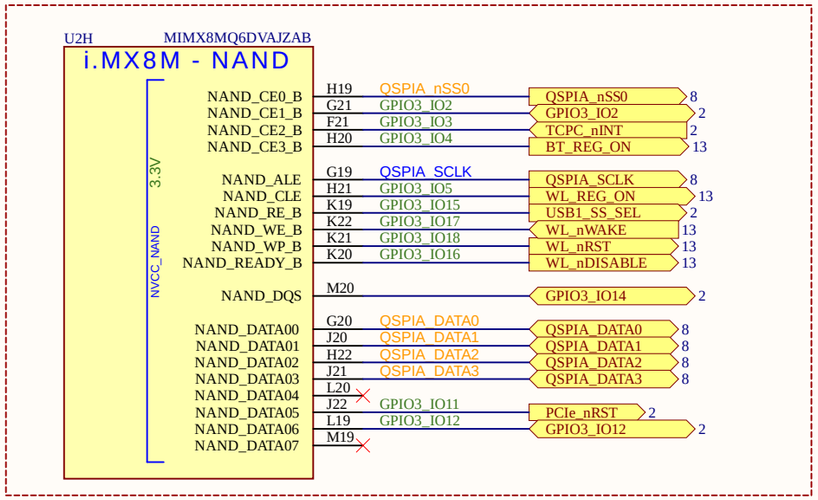
A0
A1
A2
GND
EPAD
VCC
WP
SCL
SDA

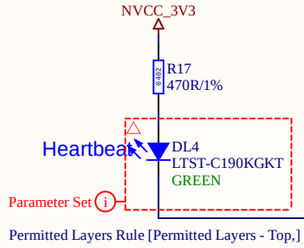
I2C2_SCL 13, 14, 15, 4, 9
I2C2_SDA 13, 14, 15, 4, 9

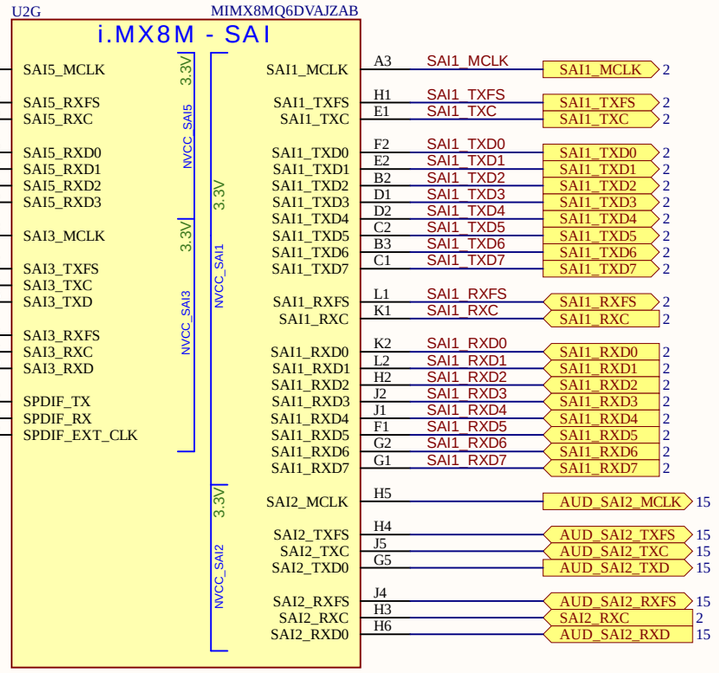
IC 24LC512-I/MF
8-DFN

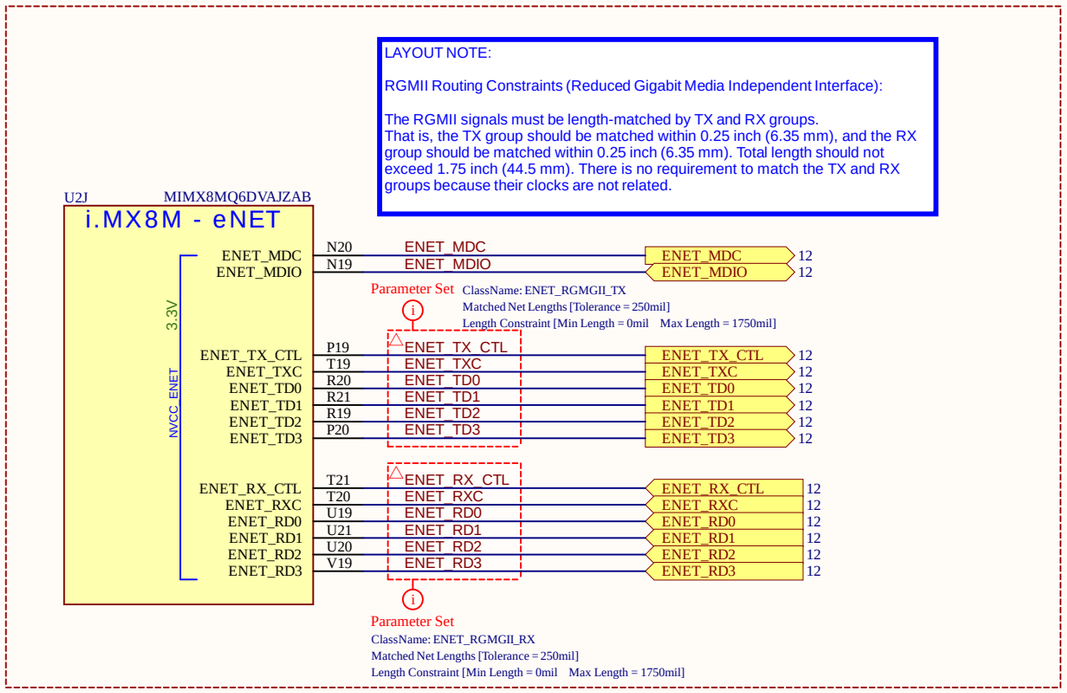
Title	eMMC, QSPI, I2C EEPROM		Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 8	Revision: 2.0	
Date: 21.09.2021	Time: 15:44:28	Sheet 8 of 16	
File: 08_EMMC_QSPI.SchDoc			

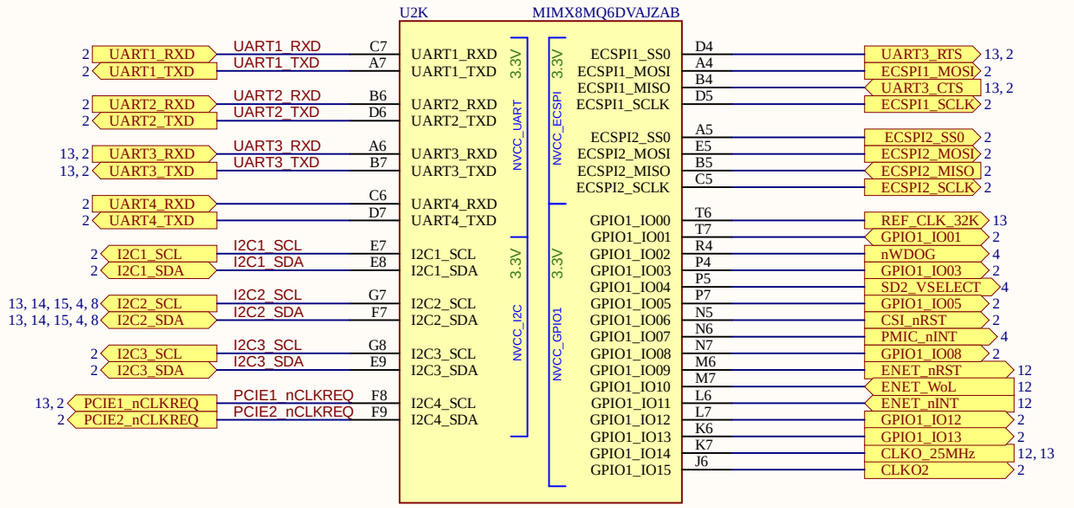
CPU - IO

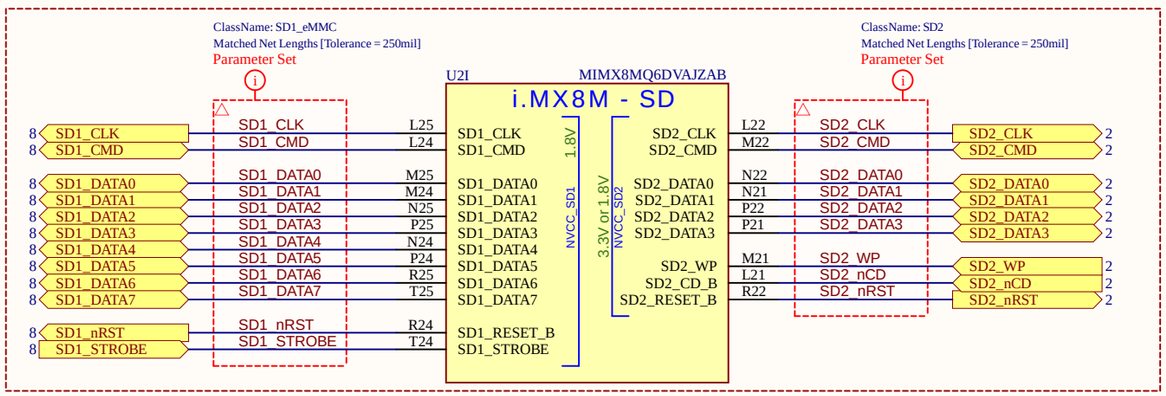


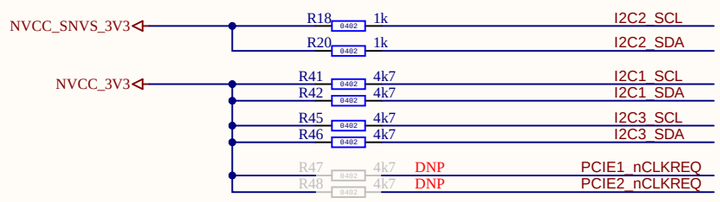












Title: CPU - IO			Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 9	Revision: 2.0	
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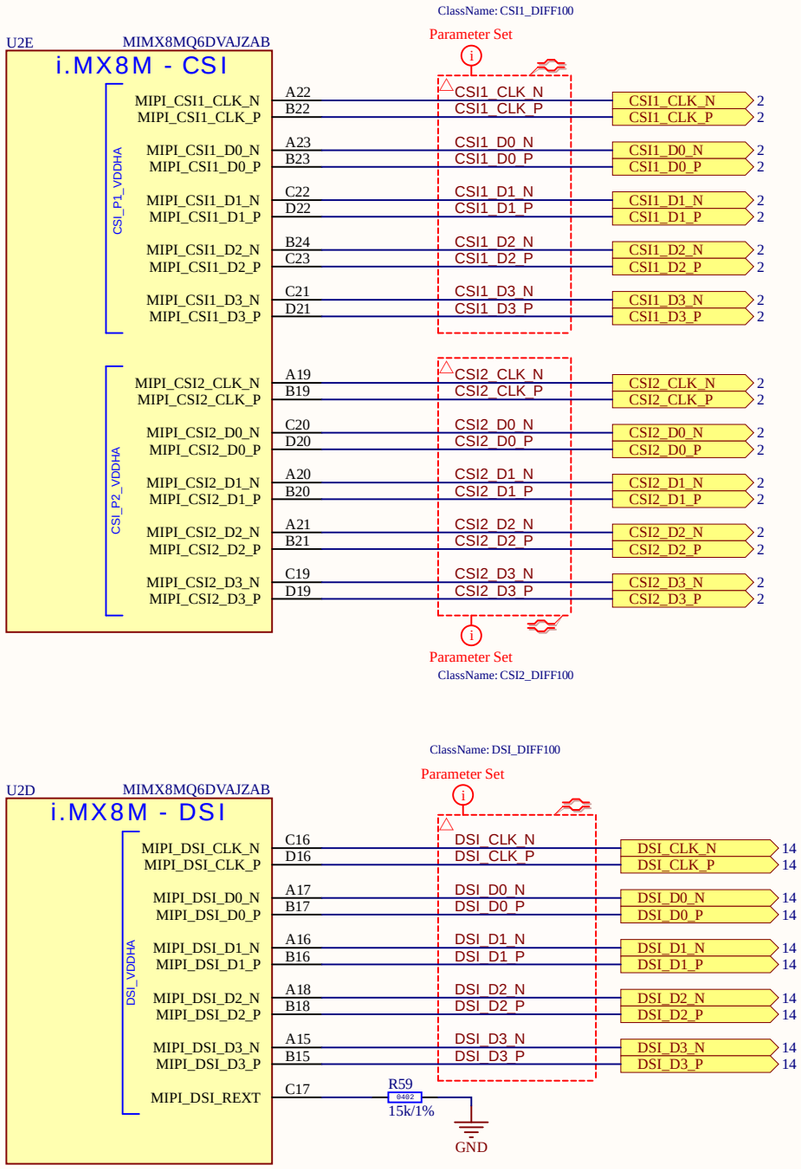
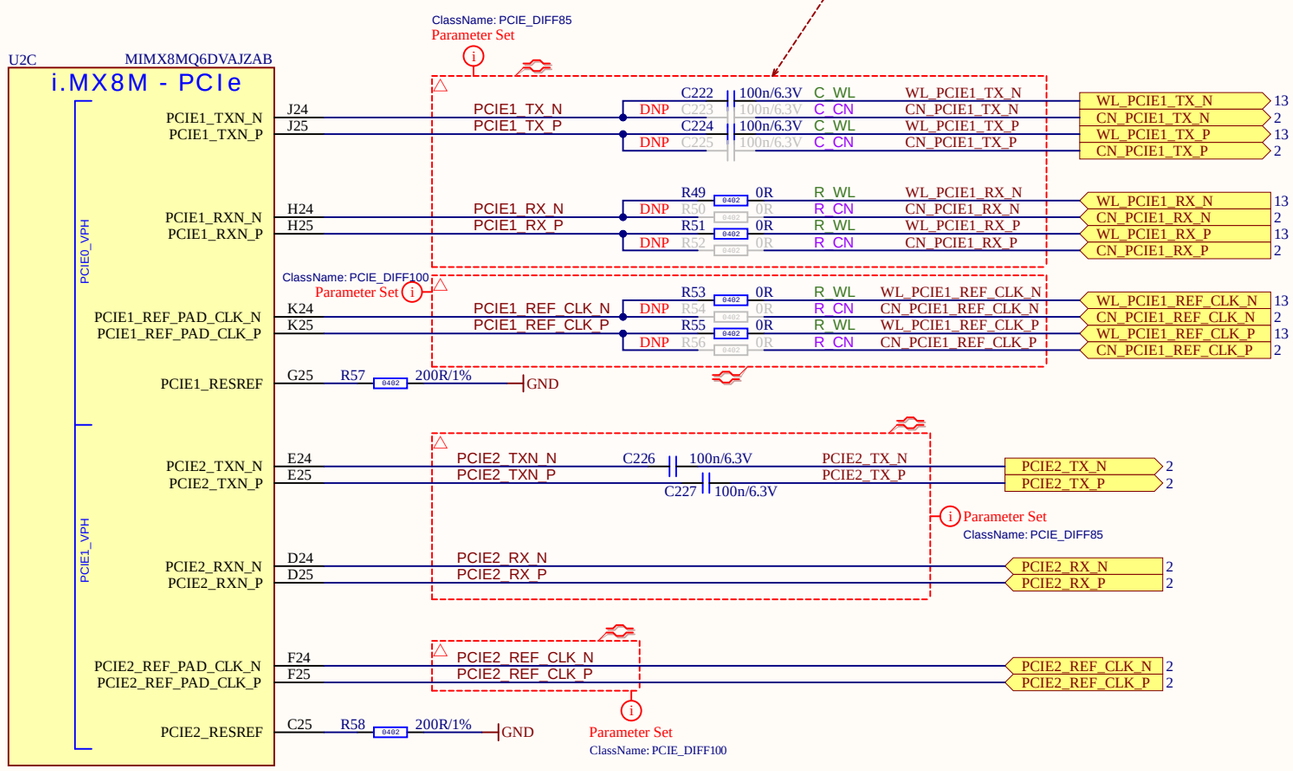
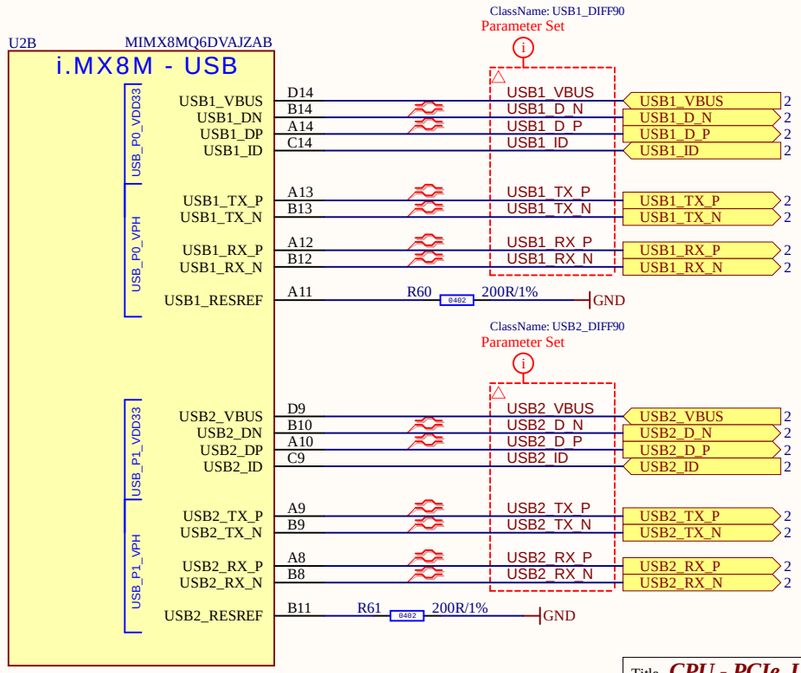
File: 09_CPU_IO.SchDoc			

RONETIX DEVELOPMENT TOOLS

CPU - PCIe, USB, DSI, CSI

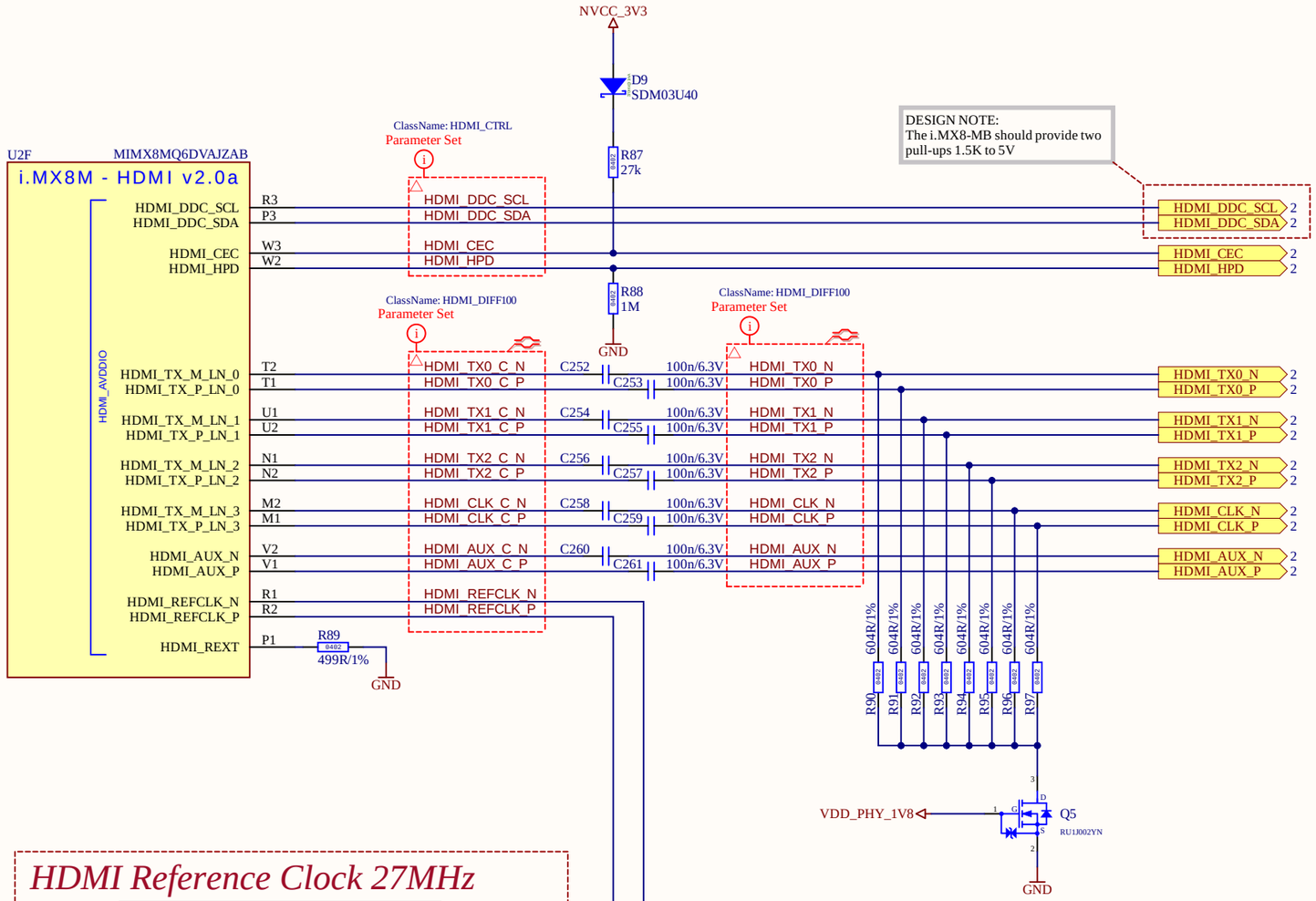


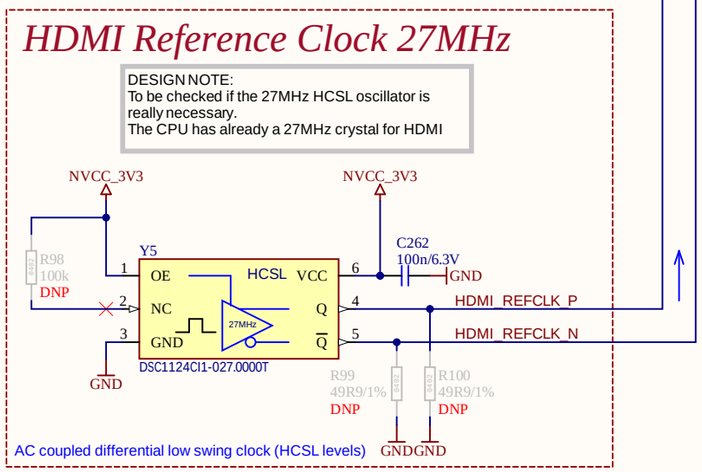




Title	CPU - PCIe, USB, DSI, CSI		Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 10	Revision: 2.0	
Date: 21.09.2021	Time: 15:44:29	Sheet 10 of 16	
File: 10_CPU_PHY.SchDoc			

CPU - HDMI





Title	CPU - HDMI		Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 11	Revision: 2.0	
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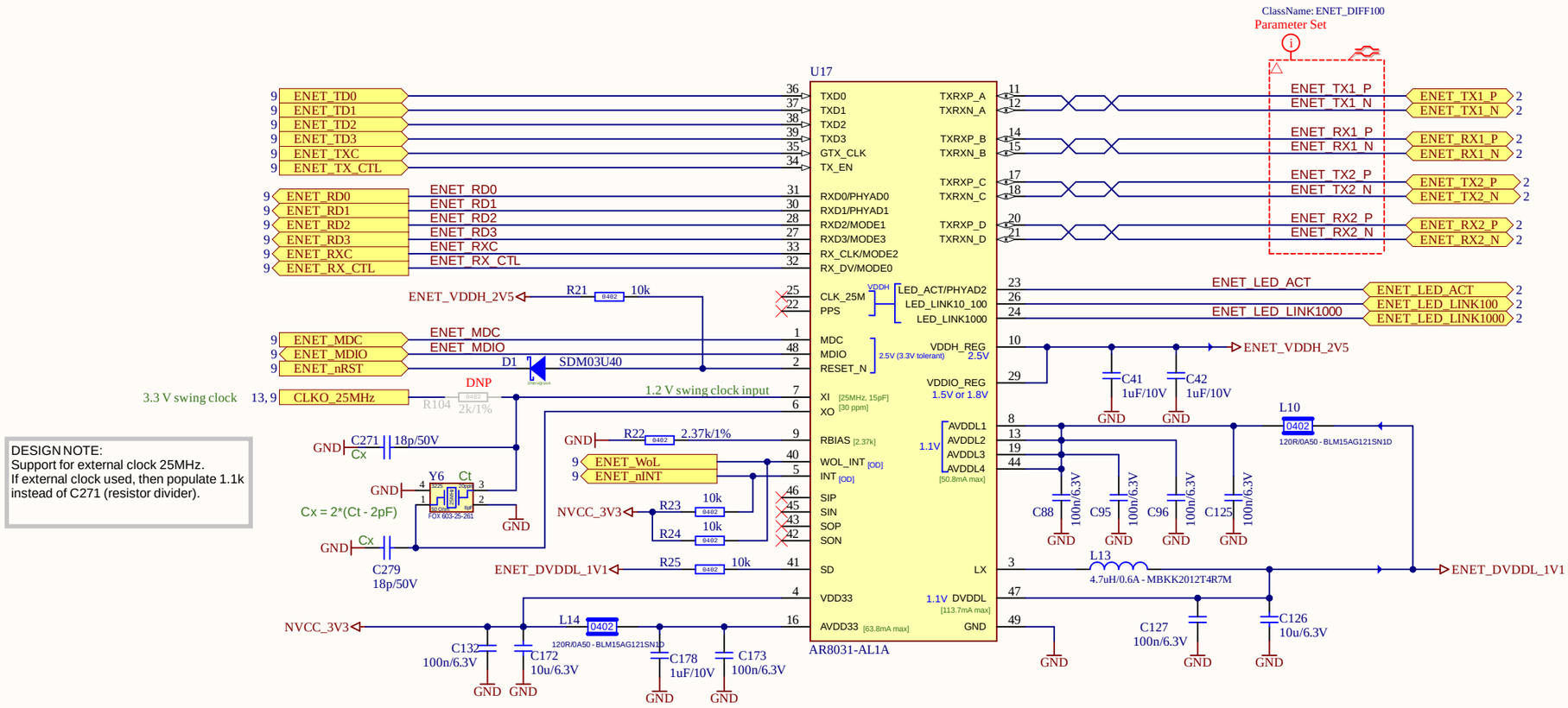
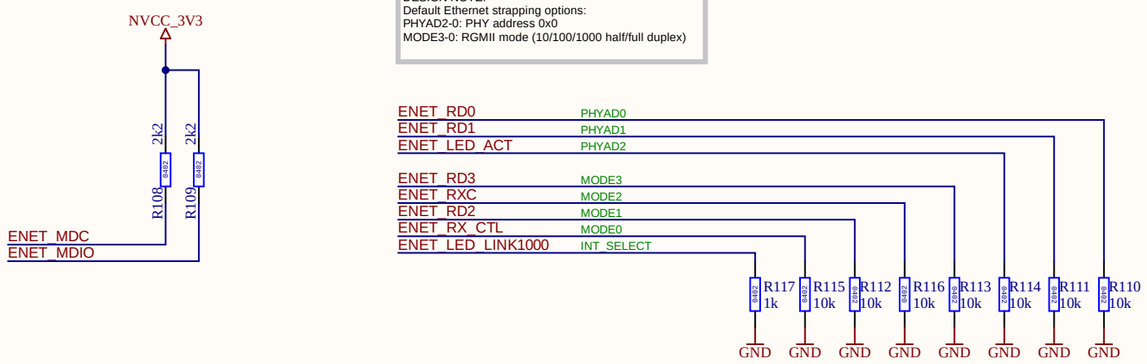
File: 11_CPU_HDMI.SchDoc			

Ethernet





Title	*Ethernet*		*Ronetix GmbH*
Size: A3	Number: 12	Revision: 2.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 15:44:29	Sheet 12 of 16	*1220 Vienna*
File: 12_ETHERNET.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

WiFi + Bluetooth

Power Consumption:
TX Mode: 610mA(avg.)
RX Mode: 285mA(avg.)

NVCC_3V3 NVCC_3V3

C236 10u/6.3V C237 100n/6.3V C238 10u/6.3V C239 100n/6.3V

GND GND GND GND

LAYOUT NOTE:
Place close to the corresponding pins of WiFi module

U4B WNSQ-261ACN(BT)

3V3_1 3V3_2 3V3_3 3V3_4

GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28

Atheros QCA6174A-5
WiFi 2x2 MIMO
802.11ac + BT 5.0

GND GND

DESIGN NOTE:
WL_REG_ON = 0 - Full Power Down

NVCC_3V3 R62 10k

WIFI_PCIE_nCLKREQ

10 WL_PCIE1_RX_P 10 WL_PCIE1_RX_N — C230 100n/6.3V — C233 100n/6.3V — 10 WL_PCIE1_TX_P 10 WL_PCIE1_TX_N

ClassName: PCIE_DIFF85
Parameter Set

WIFI_PCIE_REFCLK_P WIFI_PCIE_REFCLK_N
WL_PCIE1_RX_C_P WL_PCIE1_RX_C_N
WL_PCIE1_TX_P WL_PCIE1_TX_N

9 WL_nRST 9 WL_nWAKE 9 WL_nDISABLE

R63 100k R64 100k NVCC_3V3

2, 9 UART3_RXD 2, 9 UART3_TXD 2, 9 UART3_RTS 2, 9 UART3_CTS

R65 R66 R67 R68 0R DNP

Connecting SAI to PCM

9 BT_SAI3_TXFS 9 BT_SAI3_TXC 9 BT_SAI3_TXD 9 BT_SAI3_RXD

DNP R69 R70 R71 R74 0R

SAI3_TXFS_R SAI3_TXC_R SAI3_TXD_R SAI3_RXD_R

9 REF_CLK_32K

2 BT_USB_D_N 2 BT_USB_D_P — USB_BT_DIFF90

9 WL_REG_ON 9 BT_REG_ON

R78 100k R75 100k

U4A WNSQ-261ACN(BT)

PCIE_REFCLK_P PCIE_REFCLK_N
PCIE_TX_P PCIE_TX_N
PCIE_RX_P PCIE_RX_N
PCIE_CLKREQn [OD]
PCIE_RSTn
PCIE_WAKEn [OD]
PCIE_WL_DISABLEn

BT_UART_TXD BT_UART_RXD BT_UART_CTS BT_UART_RTS BT_UART_WAKEn [OD]

PCM_SYNC PCM_CLK PCM_IN PCM_OUT

32kHz

SDIO_DATA0 SDIO_DATA1 SDIO_DATA2 SDIO_DATA3 SDIO_CMD SDIO_CLK SDIO_WAKEn

USB_D- USB_D+

WL_REG_ON BT_REG_ON

COEX1 COEX2 COEX3 UIM_PWR_SRC UIM_PWR_SNK UIM_SWP RES1 nALERT I2C_CLK I2C_DATA SYSCLK/GNSS0 TX_BLANK/GNSS1 RES2 RES3 RES4 RES4 RES5 RES6 RES7 VENDOR1 VENDOR2 VENDOR3 RES8 RES9

WLAN_LED BT_LED

Atheros QCA6174A-5
WiFi 2x2 MIMO
802.11ac + BT 5.0

NVCC_3V3 NVCC_3V3

R72 470R/1% R73 470R/1%

DL2 LTST-C190KGKT GREEN DL3 LTST-C190KGKT GREEN

Parameter Set
Permitted Layers Rule [Permitted Layers - Top,]

DESIGN NOTE:
This component share PCB package
When use 9FGV0241 - PIN5 = GND; PIN3,7,16 = 1.8V
When use PI6CFGL201BZDIEX - PIN5 = 1.8V; PIN3,7,16 = 3.3V

VDD_1V8 NVCC_3V3

R79 DNP 0R R80 0R

L11 120R/0A50 - BLM15AG121SN1D
L12 120R/0A50 - BLM15AG121SN1D

C243 470n/6.3V C244 470n/6.3V C245 470n/6.3V

C246 470n/6.3V C247 470n/6.3V

GND

12, 9 CLKO_25MHz R81 DNP 1k R82 1k DNP

GND

6.8pF/50V C248 25MHz ±20ppm Crystal 8pF 50R Y4 C249 6.8pF/50V

FOX 603-25-261

DESIGN NOTE:
I2C address:
SADDR = 0 -> (0x68<<1)+RW
SADDR = 1 -> (0x6A<<1)+RW

14, 15, 4, 8, 9 I2C2_SCL
14, 15, 4, 8, 9 I2C2_SDA

U15 9FGV0241AKLF

X1_25 X2 SCLK_3.3 SDATA_3.3 100MHz

VDD1.8 VDD1.8 VDDDIG1.8 VDDA1.8 VDDXTAL1.8

DIF0 DIF0 DIF1 DIF1

CKPWRGD_PD 120k Pull-UP
vOE0 120k Pull-DOWN
vOE1 120k Pull-DOWN
vSS_EN_tri 120k Pull-DOWN
vSADR/REF1.8 120k Pull-DOWN

GND GND GNDDIG GNDA GNDXTAL EP(GND) GNDREF

Max 18mA

ClassName: PCIE_DIFF100
Parameter Set

WL_PCIE1_REF_CLK_P WL_PCIE1_REF_CLK_N — To CPU
WIFI_PCIE_REFCLK_P WIFI_PCIE_REFCLK_N — To WiFi module

DIFF100 DIF1_P C250 100n/6.3V
DIFF100 DIF1_N C251 100n/6.3V

DESIGN NOTE:
To support PCIe L1.1 substate, a bi-directional open drain CLKREQ# must be connected on both the Upstream and Downstream Ports of the Link

VDD_1V8 R83 100k

WIFI_PCIE_nCLKREQ D7 SDM03U40 Q4 RU1J002YN

DNP R85 0R

2, 9 PCIE1_nCLKREQ D8 SDM03U40

GND

VDD_1V8 DNP R84 0R R86 0R

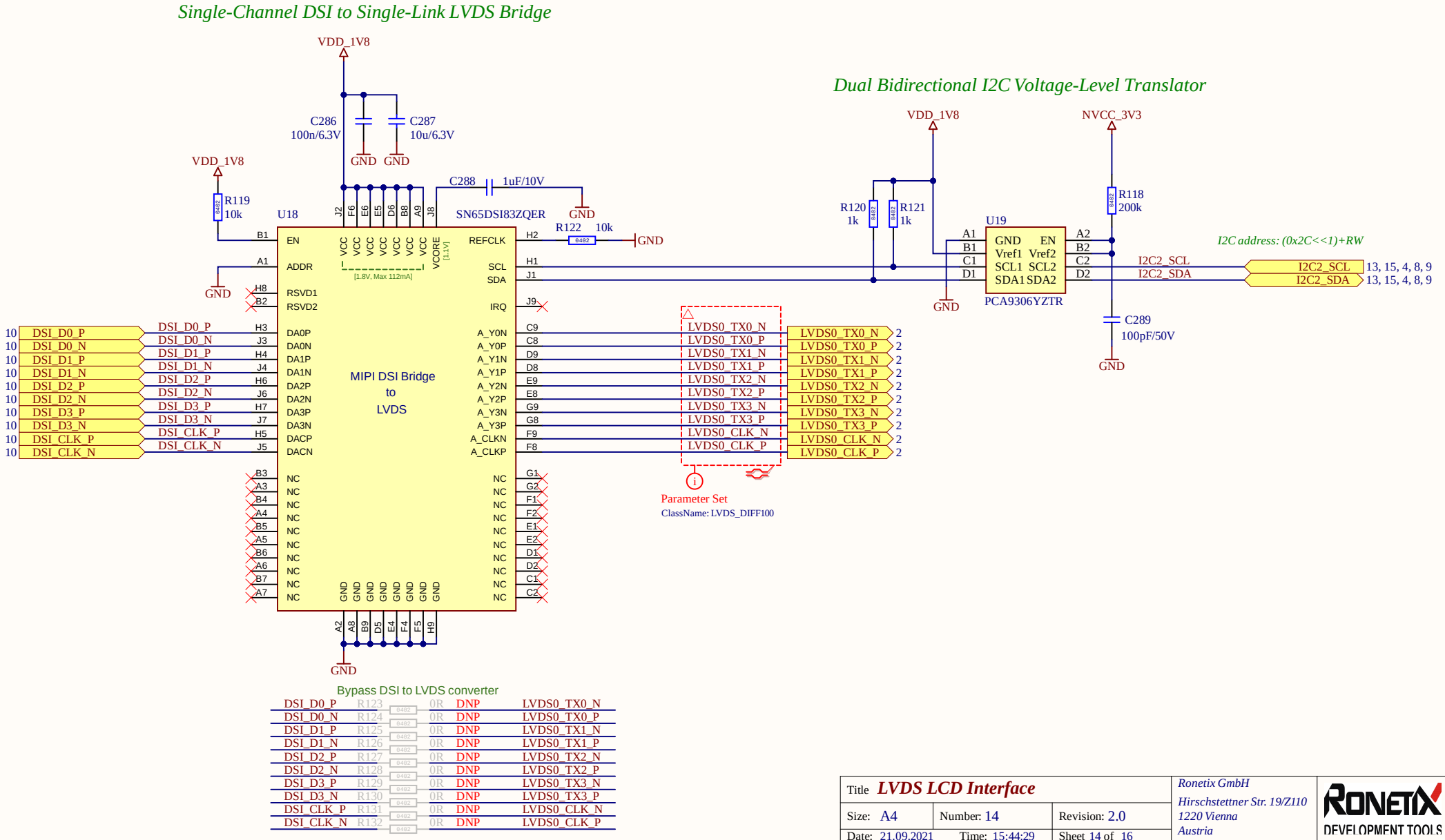
GND GND

Title	WiFi + Bluetooth		
Size: A3	Number: 13	Revision: 2.0	
Date: 21.09.2021	Time: 15:44:29	Sheet 13 of 16	
File: 13_WiFi_BT.SchDoc			

Ronetix GmbH
Hirschstettner Str. 19/Z110
1220 Vienna
Austria

RONETIX DEVELOPMENT TOOLS

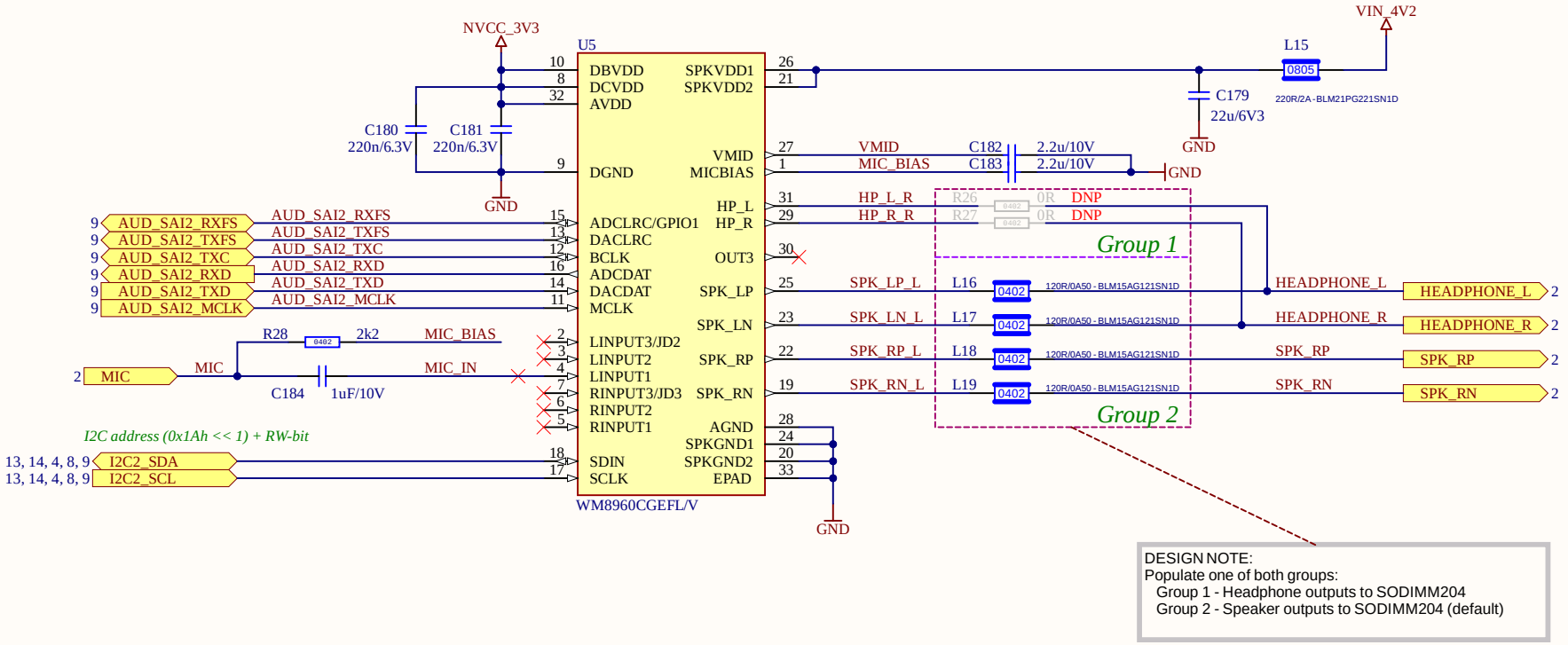
LVDS LCD Interface



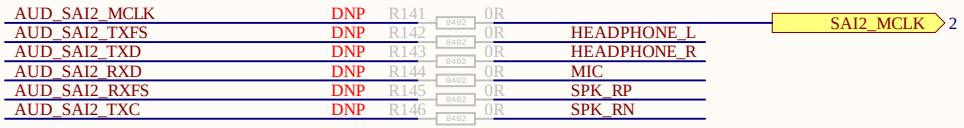
Title	*LVDS LCD Interface*		*Ronetix GmbH*
Size: A4	Number: 14	Revision: 2.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 15:44:29	Sheet 14 of 16	*1220 Vienna*
File: 14_LVDS.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

Audio Codec



DESIGN NOTE:
Populate one of both groups:
Group 1 - Headphone outputs to SODIMM204
Group 2 - Speaker outputs to SODIMM204 (default)



Title: *Audio Codec*			*Ronetix GmbH*
Size: A4	Number: 15	Revision: 2.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 15:44:29	Sheet 15 of 16	*1220 Vienna*
File: 15_Audio.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Alt6 Special EN	ALT7	Alt7 Special EN
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									
BOOT_MODE0	ccmsrcgpcmix.BOOT_MODE[0]	ccmsrcgpcmix.BOOT_MODE[0]									
BOOT_MODE1	ccmsrcgpcmix.BOOT_MODE[1]	ccmsrcgpcmix.BOOT_MODE[1]									
JTAG_MOD	cjtag_wrapper.MOD	cjtag_wrapper.MODE									
JTAG_TRST_B	cjtag_wrapper.TRST_B	cjtag_wrapper.TRST_B									
JTAG_TDI	cjtag_wrapper.TDI	cjtag_wrapper.TDI									
JTAG_TMS	cjtag_wrapper.TMS	cjtag_wrapper.TMS									
JTAG_TCK	cjtag_wrapper.TCK	cjtag_wrapper.TCK									
JTAG_TDO	cjtag_wrapper.TDO	cjtag_wrapper.TDO									
RTC	snvsmix.RTC	snvsmix.RTC									
PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ									
PMIC_ON_REQ	snvsmix.PMIC_ON_REQ	snvsmix.PMIC_ON_REQ									
ONOFF	snvsmix.ONOFF	snvsmix.ONOFF									
POR_B	snvsmix.POR_B	snvsmix.POR_B									
RTC_RESET_B	snvsmix.RTC_POR_B	snvsmix.RTC_RESET_B									
GPIO1_IO00	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT					ccmsrcgpcmix.EXT_CLK1		sjc.FAIL	
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT					ccmsrcgpcmix.EXT_CLK2		sjc.ACTIVE	ccmsrcgpcmix.src_system_rst
GPIO1_IO02	gpio1.IO[2]	gpio1.IO[2]	wdog1.WDOG_B							sjc.DE_B	sjc.sjc_gpucr1_reg[30]
GPIO1_IO03	gpio1.IO[3]	gpio1.IO[3]	usdhc1.VSELECT					anamix.xtal_ok		sjc.DONE	
GPIO1_IO04	gpio1.IO[4]	gpio1.IO[4]	usdhc2.VSELECT					anamix.xtal_ok_lv		usdhc1.TEST_TRIG	
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				anamix.REF_CLK_32K	ccmsrcgpcmix.INT_BOOT	ccmsrcgpcmix.src_system_rst	usdhc2.TEST_TRIG	
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				anamix.REF_CLK_24M	ccmsrcgpcmix.EXT_CLK3		ecspi1.TEST_TRIG	
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				wdog1.WDOG_ANY	ccmsrcgpcmix.EXT_CLK4		ecspi2.TEST_TRIG	
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				sdma1.EXT_EVENT[0]	ccmsrcgpcmix.WAIT		qspi.TEST_TRIG	
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT				sdma1.EXT_EVENT[1]	ccmsrcgpcmix.STOP		rawnand.TEST_TRIG	
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]	usb1.OTG_ID				ccmsrcgpcmix.PMIC_READY			ocotp_ctrl_wrapper.FUSE_LATCHED	sjc.sjc_gpucr3_reg[14]
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	usb2.OTG_ID				usdhc1.CD_B	ccmsrcgpcmix.OUT0		caam_wrapper.RNG_OSC_OBS	
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				usdhc1.WP	ccmsrcgpcmix.OUT1		csu.CSU_ALARM_AUT[0]	
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				usdhc2.RESET_B	ccmsrcgpcmix.OUT2		csu.CSU_ALARM_AUT[1]	
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR				sdma2.EXT_EVENT[0]	ccmsrcgpcmix.CLKO1		csu.CSU_ALARM_AUT[2]	
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC					ccmsrcgpcmix.CLKO2		csu.CSU_INT_DEB	
ENET_MDC	gpio1.IO[16]	enet1.MDC					ccmsrcgpcmix.PMIC_READY				
ENET_MDIO	gpio1.IO[17]	enet1.MDIO					sdma2.EXT_EVENT[1]				
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3					pwm2.OUT				
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	"INPUT=enet1.TX_CLK				pwm3.OUT				
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1	OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT"				pwm4.OUT				
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0					gpio1.IO[16]				
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL					gpio1.IO[17]				
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC	enet1.TX_ER				gpio1.IO[18]				
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL					gpio1.IO[19]				
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC	enet1.RX_ER				gpio1.IO[20]				
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0					gpio1.IO[21]				
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1					gpio1.IO[22]				
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2					gpio1.IO[23]				
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3					gpio1.IO[24]				
SD1_CLK	gpio2.IO[0]	usdhc1.CLK					gpio1.IO[25]				
SD1_CMD	gpio2.IO[1]	usdhc1.CMD					gpio1.IO[26]				
SD1_DATA0	gpio2.IO[2]	usdhc1.DATA0					gpio1.IO[27]				
SD1_DATA1	gpio2.IO[3]	usdhc1.DATA1					gpio1.IO[28]				
SD1_DATA2	gpio2.IO[4]	usdhc1.DATA2					gpio1.IO[29]				
SD1_DATA3	gpio2.IO[5]	usdhc1.DATA3					gpio2.IO[0]				
SD1_DATA4	gpio2.IO[6]	usdhc1.DATA4					gpio2.IO[1]	ccmsrcgpcmix.OBSERVE0		observe_mux.OUT[0]	
SD1_DATA5	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[2]	ccmsrcgpcmix.OBSERVE1		observe_mux.OUT[1]	
SD1_DATA6	gpio2.IO[8]	usdhc1.DATA6					gpio2.IO[3]	ccmsrcgpcmix.OBSERVE2		observe_mux.OUT[2]	
SD1_DATA7	gpio2.IO[9]	usdhc1.DATA7					gpio2.IO[4]	ccmsrcgpcmix.WAIT		observe_mux.OUT[3]	
SD1_RESET_B	gpio2.IO[10]	usdhc1.RESET_B					gpio2.IO[5]	ccmsrcgpcmix.STOP		observe_mux.OUT[4]	
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[6]	ccmsrcgpcmix.EARLY_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[7]	ccmsrcgpcmix.SYSTEM_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_CLK	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[8]				
SD2_CMD	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[9]			sim_m.HMASTLOCK	sjc.sjc_gpucr1_reg[11]
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[10]			sim_m.HPROT[0]	sjc.sjc_gpucr1_reg[11]
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[11]			sim_m.HPROT[1]	sjc.sjc_gpucr1_reg[11]
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[12]			sim_m.HPROT[2]	sjc.sjc_gpucr1_reg[11]
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[13]			sim_m.HPROT[3]	sjc.sjc_gpucr1_reg[11]
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[14]			sim_m.HSIZE[0]	sjc.sjc_gpucr1_reg[11]
SD2_WP	gpio2.IO[20]	usdhc2.WP					gpio2.IO[15]			sim_m.HADDR[1]	sjc.sjc_gpucr1_reg[11]
NAND_ALE	gpio3.IO[0]	rawnand.ALE	qspi.A_SCLK				gpio2.IO[16]			sim_m.HADDR[2]	sjc.sjc_gpucr1_reg[11]
NAND_CE0_B	gpio3.IO[1]	rawnand.CE0_B	qspi.A_SS0_B				gpio2.IO[17]			sim_m.HADDR[3]	sjc.sjc_gpucr1_reg[11]
NAND_CE1_B	gpio3.IO[2]	rawnand.CE1_B	qspi.A_SS1_B				gpio2.IO[18]			sim_m.HADDR[4]	sjc.sjc_gpucr1_reg[11]
NAND_CE2_B	gpio3.IO[3]	rawnand.CE2_B	qspi.B_SS0_B				gpio2.IO[19]			sim_m.HADDR[5]	sjc.sjc_gpucr1_reg[11]
NAND_CE3_B	gpio3.IO[4]	rawnand.CE3_B	qspi.B_SS1_B				gpio2.IO[20]			sim_m.HADDR[6]	sjc.sjc_gpucr1_reg[11]
NAND_CLE	gpio3.IO[5]	rawnand.CLE	qspi.B_SCLK				gpio3.IO[0]			sim_m.HADDR[7]	sjc.sjc_gpucr1_reg[11]
NAND_DATA00	gpio3.IO[6]	rawnand.DATA00	qspi.A_DATA[0]				gpio3.IO[1]			sim_m.HADDR[8]	sjc.sjc_gpucr1_reg[11]
NAND_DATA01	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[2]			sim_m.HADDR[9]	sjc.sjc_gpucr1_reg[11]
NAND_DATA02	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[2]				gpio3.IO[3]			sim_m.HADDR[10]	sjc.sjc_gpucr1_reg[11]
NAND_DATA03	gpio3.IO[9]	rawnand.DATA03	qspi.A_DATA[3]				gpio3.IO[4]			sim_m.HADDR[11]	sjc.sjc_gpucr1_reg[11]
NAND_DATA04	gpio3.IO[10]	rawnand.DATA04	qspi.B_DATA[0]				gpio3.IO[5]			sim_m.HADDR[12]	sjc.sjc_gpucr1_reg[11]
NAND_DATA05	gpio3.IO[11]	rawnand.DATA05	qspi.B_DATA[1]				gpio3.IO[6]			sim_m.HADDR[13]	sjc.sjc_gpucr1_reg[11]
NAND_DATA06	gpio3.IO[12]	rawnand.DATA06	qspi.B_DATA[2]				gpio3.IO[7]	ccmsrcgpcmix.TESTER_ACK	ccmsrcgpcmix.src_en_system_clk	sim_m.HADDR[14]	sjc.sjc_gpucr1_reg[11]
NAND_DATA07	gpio3.IO[13]	rawnand.DATA07	qspi.B_DATA[3]				gpio3.IO[8]			sim_m.HADDR[15]	sjc.sjc_gpucr1_reg[11]
NAND_DQS	gpio3.IO[14]	rawnand.DQS	qspi.A_DQS				gpio3.IO[9]	ccmsrcgpcmix.BOOT_CFG[0]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[16]	sjc.sjc_gpucr1_reg[11]
NAND_RE_B	gpio3.IO[15]	rawnand.RE_B	qspi.B_DQS				gpio3.IO[10]	ccmsrcgpcmix.BOOT_CFG[1]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[17]	sjc.sjc_gpucr1_reg[11]
NAND_READY_B	gpio3.IO[16]	rawnand.READY_B					gpio3.IO[11]	ccmsrcgpcmix.BOOT_CFG[2]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[18]	sjc.sjc_gpucr1_reg[11]
NAND_WE_B	gpio3.IO[17]	rawnand.WE_B					gpio3.IO[12]	ccmsrcgpcmix.BOOT_CFG[3]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[19]	sjc.sjc_gpucr1_reg[11]
NAND_WP_B	gpio3.IO[18]	rawnand.WP_B					gpio3.IO[13]	ccmsrcgpcmix.BOOT_CFG[4]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[20]	sjc.sjc_gpucr1_reg[11]
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]	sai1.TX_SYNC	sai5.TX_SYNC		gpio3.IO[14]	ccmsrcgpcmix.BOOT_CFG[5]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[21]	sjc.sjc_gpucr1_reg[11]
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	sai1.TX_DATA[1]	sai1.TX_SYNC	sai5.TX_BCLK		gpio3.IO[15]	ccmsrcgpcmix.BOOT_CFG[6]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[22]	sjc.sjc_gpucr1_reg[11]
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]	sai1.TX_SYNC	sai5.TX_DATA[0]		gpio3.IO[16]	ccmsrcgpcmix.BOOT_CFG[7]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[23]	sjc.sjc_gpucr1_reg[11]
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC			gpio3.IO[17]			sim_m.HADDR[24]	sjc.sjc_gpucr1_reg[11]
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_SYNC			gpio3.IO[18]	ccmsrcgpcmix.BOOT_CFG[8]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[25]	sjc.sjc_gpucr1_reg[11]
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai4.MCLK			gpio3.IO[19]	ccmsrcgpcmix.BOOT_CFG[9]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[26]	sjc.sjc_gpucr1_reg[11]
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[20]	ccmsrcgpcmix.BOOT_CFG[10]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[27]	sjc.sjc_gpucr1_reg[11]
SAI1_RXFS	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio3.IO[21]	ccmsrcgpcmix.BOOT_CFG[11]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[28]	sjc.sjc_gpucr1_reg[11]
SAI1_RXC	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio3.IO[22]	ccmsrcgpcmix.BOOT_CFG[12]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[29]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD0	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]			coresight.TRACE[0]	gpio3.IO[23]	ccmsrcgpcmix.BOOT_CFG[13]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[30]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD1	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]			coresight.TRACE[1]	gpio3.IO[24]	ccmsrcgpcmix.BOOT_CFG[14]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[31]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD2	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]			coresight.TRACE[2]	gpio3.IO[25]	ccmsrcgpcmix.BOOT_CFG[15]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[0]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD3	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]			coresight.TRACE[3]	gpio4.IO[0]			sim_m.HBURST[1]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD4	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.RX_BCLK			coresight.TRACE[4]	gpio4.IO[1]			sim_m.HBURST[2]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD5	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.RX_DATA[0]			coresight.TRACE[5]	gpio4.IO[2]			sim_m.HRESP	sjc.sjc_gpucr1_reg[11]
SAI1_RXD6	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.RX_SYNC			coresight.TRACE[6]	gpio4.IO[3]			sim_m.HSIZE[0]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD7	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK			coresight.TRACE[7]	gpio4.IO[4]			sim_m.HSIZE[1]	sjc.sjc_gpucr1_reg[11]
SAI1_TXFS	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[5]			sim_m.HSIZE[2]	sjc.sjc_gpucr1_reg[11]
SAI1_TXC	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENTI	gpio4.IO[6]			sim_m.HWRITE	sjc.sjc_gpucr1_reg[11]
SAI1_TXD0	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[7]			sim_m.HREADYOUT	sjc.sjc_gpucr1_reg[11]
SAI1_TXD1	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[8]			tpsmp.CLK	sjc.sjc_gpucr1_reg[11]
SAI1_TXD2	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[9]			tpsmp.HDATA_DIR	sjc.sjc_gpucr1_reg[11]
SAI1_TXD3	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[10]			tpsmp.HTRANS[0]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD4	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.TX_BCLK			coresight.TRACE[12]	gpio4.IO[11]			tpsmp.HTRANS[1]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD5	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.TX_DATA[0]			coresight.TRACE[13]	gpio4.IO[12]			tpsmp.HDATA[0]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD6	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.TX_SYNC			coresight.TRACE[14]	gpio4.IO[13]			tpsmp.HDATA[1]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD7	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK			coresight.TRACE[15]	gpio4.IO[14]			tpsmp.HDATA[2]	sjc.sjc_gpucr1_reg[11]
SAI1_MCLK	gpio4.IO[20]	sai1.MCLK	sai5.MCLK				gpio4.IO[15]			tpsmp.HDATA[3]	sjc.sjc_gpucr1_reg[11]
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC				gpio4.IO[16]			tpsmp.HDATA[4]	sjc.sjc_gpucr1_reg[11]
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK				gpio4.IO[17]			tpsmp.HDATA[5]	sjc.sjc_gpucr1_reg[11]
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_DATA[0]				gpio4.IO[18]			tpsmp.HDATA[6]	sjc.sjc_gpucr1_reg[11]
SAI2_TXFS	gpio4.IO[24]	sai2.TX_SYNC	sai5.TX_DATA[1]				gpio4.IO[19]			tpsmp.HDATA[7]	sjc.sjc_gpucr1_reg[11]
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[2]				gpio4.IO[20]			tpsmp.HDATA[8]	sjc.sjc_gpucr1_reg[11]
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[3]				gpio4.IO[21]			tpsmp.HDATA[9]	sjc.sjc_gpucr1_reg[11]
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.MCLK				gpio4.IO[22]			tpsmp.HDATA[10]	sjc.sjc_gpucr1_reg[11]
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC			gpio4.IO[23]			tpsmp.HDATA[11]	sjc.sjc_gpucr1_reg[11]
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CAPTURE2	sai5.RX_BCLK			gpio4.IO[24]			tpsmp.HDATA[12]	sjc.sjc_gpucr1_reg[11]
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]			gpio4.IO[25]			tpsmp.HDATA[13]	sjc.sjc_gpucr1_reg[11]
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CLK	sai5.RX_DATA[1]			gpio4.IO[26]			tpsmp.HDATA[14]	sjc.sjc_gpucr1_reg[11]
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]			gpio4.IO[27]			tpsmp.HDATA[15]	sjc.sjc_gpucr1_reg[11]
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio4.IO[28]			tpsmp.HDATA[16]	sjc.sjc_gpucr1_reg[11]
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio4.IO[29]			tpsmp.HDATA[17]	sjc.sjc_gpucr1_reg[11]
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio4.IO[30]			tpsmp.HDATA[18]	sjc.sjc_gpucr1_reg[11]
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio4.IO[31]			tpsmp.HDATA[19]	sjc.sjc_gpucr1_reg[11]
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[0]			tpsmp.HDATA[20]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SCLK	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[1]			tpsmp.HDATA[21]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MOSI	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[2]			tpsmp.HDATA[22]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MISO	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[3]			tpsmp.HDATA[23]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SS0	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[4]			tpsmp.HDATA[24]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[5]			tpsmp.HDATA[25]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[6]			tpsmp.HDATA[26]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[7]			tpsmp.HDATA[27]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[8]			tpsmp.HDATA[28]	sjc.sjc_gpucr1_reg[11]
I2C1_SCL	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[9]			tpsmp.HDATA[29]	sjc.sjc_gpucr1_reg[11]
I2C1_SDA	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[10]			tpsmp.HDATA[30]	sjc.sjc_gpucr1_reg[11]
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.1588_EVENT1_IN				gpio5.IO[11]			tpsmp.HDATA[31]	sjc.sjc_gpucr1_reg[11]
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_EVENT1_OUT				gpio5.IO[12]				
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[13]				
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[14]				
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[15]				
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm1.OUT	pcie2.CLKREQ_B			gpio5.IO[16]				
UART1_RXD	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[17]				
UART1_TXD	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[18]				
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[19]				
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[20]				
UART3_RXD	gpio5.IO[26]	uart3.RX	uart1.CTS_B				gpio5.IO[21]				
UART3_TXD	gpio5.IO[27]	uart3.TX	uart1.RTS_B				gpio5.IO[22]				
UART4_RXD	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[23]				
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.RTS_B	pcie2.CLKREQ_B			gpio5.IO[24]				

PIN MUX

Title	PIN MUX		
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