RONETIX
DEVELOPMENT TOOLS

# i.MX8M-CM

CPU Module (SoM) with NXP i.MX8MQ

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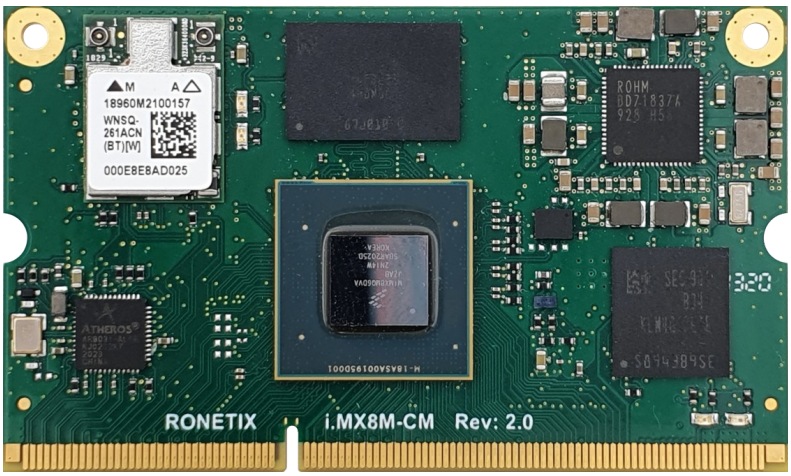
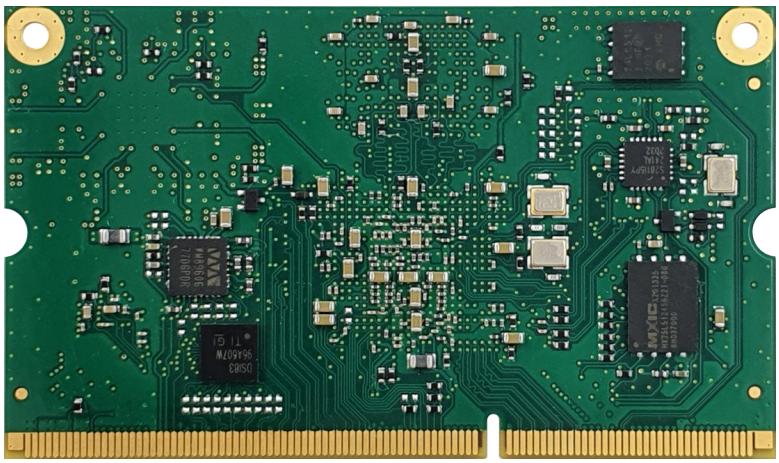
Datasheet

rev 1.0



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# 1. Document Revision History

| Revision | Date | Notes |
|---|---|---|
| 1.0 | 01-Jun-2021 | Initial release |
| | | |

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# 3. Overview

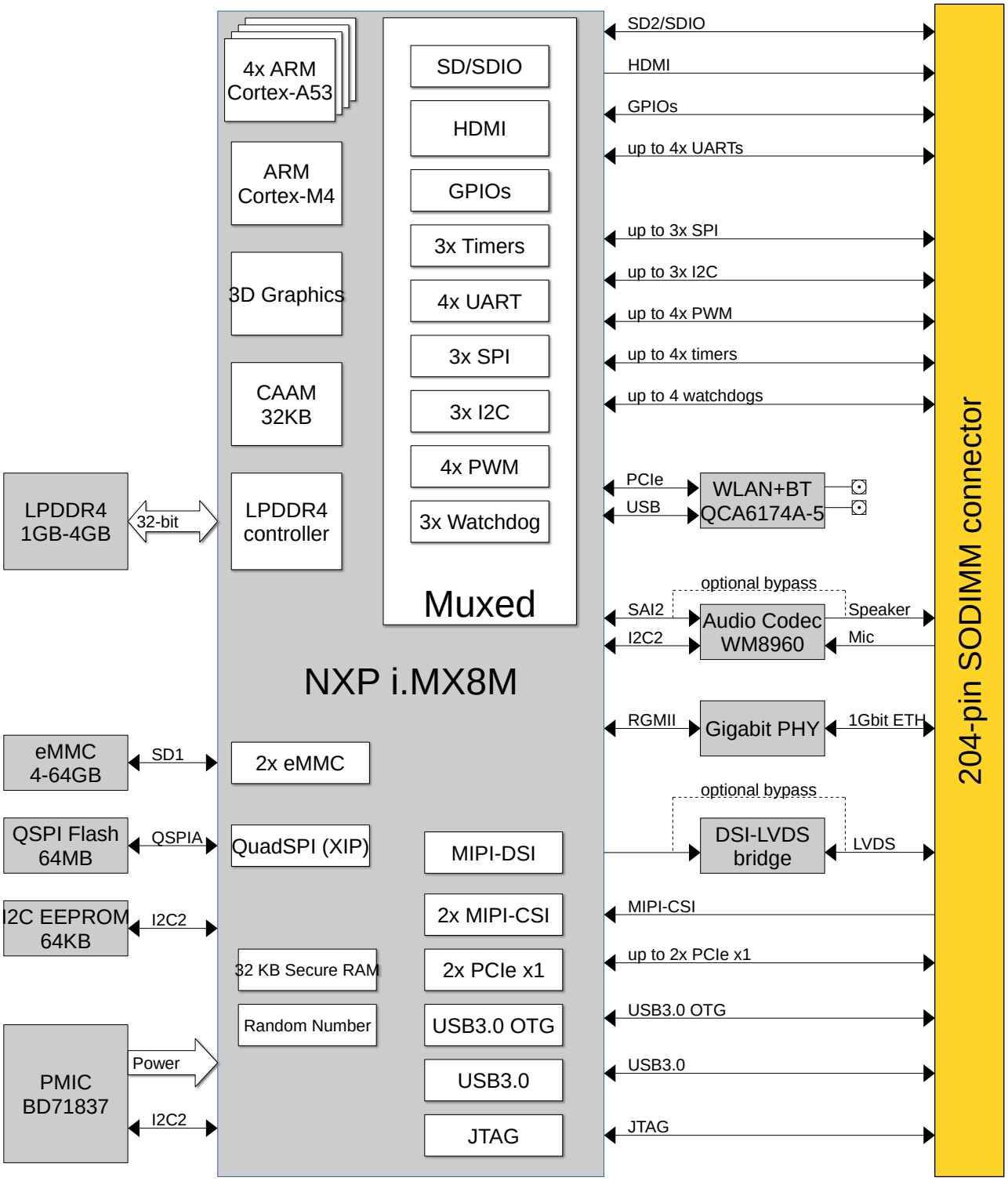
## 3.1 General Information

The **i.MX8M-CM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX8MQ family of multipurpose processors from which feature an ARM® Cortex™-A53 up to 1.5GHz + an additional ARM Cortex-M4. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

## 3.2 Highlights

| | |
|---|---|
| CPU | • Quad Armv8-A, 64-bit Cortex™-A53 Core, 1.5GHz<br>• ARM® Cortex™-M4, 266MHz |
| Memory | • RAM: 1 GiB LPDDR4 (optional: up to 4 GiB)<br>• eMMC: 4 GiB (optional: up to 64 GiB)<br>• I2C EEPROM: 64KiB (optional)<br>• QSPI NOR Flash: 64 MiB (optional) |
| Display | • HDMI<br>• LVDS, up to 1400 x 1050 @60Hz<br>• MIPI DSI |
| Camera | • 2x MIPI-CSI, 4 data lanes |
| Network | • Ethernet: 10/100/1000Mbps<br>• WiFi: Atheros QCA6174A-5, 802.11ac, dual band 2×2 MIMO (optional)<br>• Bluetooth: Bluetooth 5.0 Secure Connection Compliant (optional) |
| Audio | • Audio codec WM8960: Stereo Headphone, Stereo Class D Speaker 1W, Microphone |
| I/O | • 2x PCIe 2.0, 1-lane each<br>• 2x USB3.0/2.0 OTG port<br>• Up to 4x UART ports<br>• MMC/SD/SDIO<br>• Up to 3x SPI<br>• Up to 3x I2C<br>• Up to 4x general purpose PWM signals<br>• GPIOs |
| Electrical | • Supply Voltage: 3.5 – 4.5V |
| Physical | • Board size: 67x40mm<br>• SO-DIMM 200 JEDEC MO-274 module (67.6x40mm)<br>• Operation temperature: 0° +70°C, -20° to 85° C (optional)<br>• Relative humidity: 10% to 90%<br>• MTTF > 200000 hours |

## 3.3 Block Diagram



# 4. CPU Module Hardware Components

This chapter describes the hardware components of i.MX8M-CM SoM.

## 4.1 Power supply

i.MX8M-CM uses Rohm's BD71837 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M series of application processors. The PMIC regulates all power rails required on CPU module from a single 3.8V-5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

## 4.2 CPU i.MX8MQ

The i.MX 8M Dual / 8M Quad processors represent NXP's latest market of connected streaming audio/video devices, scanning/imaging devices, and various devices requiring high-performance, low-power processors. The i.MX 8M Dual / 8M Quad processors feature advanced implementation of a quad Arm®Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M4 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3Lmemory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

### 4.2.1 Block Diagram

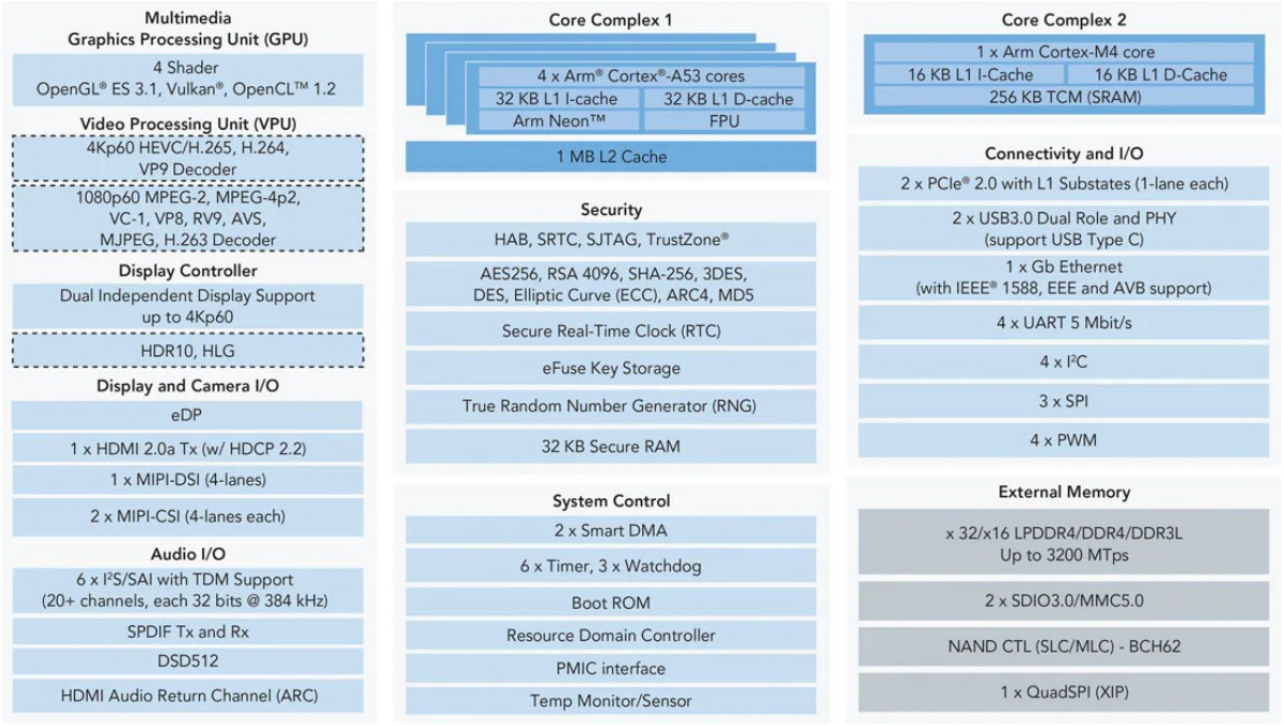



*Figure 4.1: iMX8M Block Diagram*

### 4.2.2 CPU Platform

The i.MX8M Quad processor implements four ARM® Cortex®-A53 cores intended for high level O/S, with an ARM® Cortex®-M4 core dedicated for real-time tasks.

The ARM Cortex-A53 MPCore™ platform has the following features:

- Quad ARM Cortex-A53 Cores
- Target frequency of 1.5GHz
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - MPE (media processing engine) with NEON co-processor supporting SIMD architecture
- The Arm Cortex-A53 Core complex shares:

- General interrupt controller (GIC) with 128 interrupt support
- Global timer
- Snoop control unit (SCU)
- 1 MB unified I/D L2 cache
- NEON MPE co-processor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The ARM Cortex-M4 platform includes the following features:

- Cortex-M4 CPU core operating at 266 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 256 KByte TCM (tightly-coupled memory)

## 4.3 Memory

### 4.3.1 DRAM

i.MX8M-CM is standard equipped with 1 GB LPDDR4 memory. Optionally up to 4 GB can be assembled. The data bus is 32-bit wide.

### 4.3.2 eMMC – non-volatile storage memory

i.MX8M-CM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

### 4.3.3 SPI NOR Flash

i.MX8M-CM can be assembled with a QSPI NOR Flash.

### 4.3.4 I2C EEPROM

i.MX8M-CM can be assembled with a I2C EEPROM.

## 4.4 Gigabit Ethernet

i.MX8M-CM implements one full-featured 10/100/1000 Ethernet ports implemented with MAC built into the i.MX8M SoC, coupled with AR8031 RGMII Ethernet PHYs from Qualcomm. The Ethernet interface support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

## 4.5 WLAN

i.MX8M-CM optional wireless communication is implemented with SparkLAN WNSQ-261ACN(BT) WLAN module. WNSQ-261ACN(BT) is an 802.11ac/b/g/n Dual-Band Wi-Fi+Bluetooth M.2 LGA type 1216 module based on Qualcomm Atheros QCA6174A-5 chipset. It is Dual-Band AC on 2.4GHz + 5GHz and incorporates the latest Bluetooth 5.0. The download speed are 300Mbps on N networks and 867Mbps on AC network.

i.MX8M-CM is equipped with two U.FL high frequency connectors for external antennas.

## 4.6 Audio

i.MX8M-CM implements an audio codec WM8960 (assembled optional) . The WM8960 is a low power stereo codec featuring Class D speaker drivers to provide 1W per channel into 8Ω loads. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input. Stereo 24-bit Delta Sigma converters are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio

interface. The main clock can be input directly or generated internally by an onboard PLL, supporting most commonly used clocking schemes.

The WM8960 supports the following features:

- Stereo class D speaker driver, 1W per channel
- On-chip headphone driver 40mW output power into 16Ω
- Microphone interface
- Pop and click suppression
- DAC SNR 98 dB ('A' weighted), THD -84 dB at 48 kHz, 3.3V
- ADC SNR 95 dB ('A' weighted),THD -82 dB at 48 kHz, 3.3V
- Programmable ALC / limiter and noise gate

Please refer to the WM8960 datasheet for additional details.

## 4.7 LVDS bridge

i.MX8M-CM implements (optional) onboard LVDS display interface by converting the MIPI-DSI to LVDS signals using Texas Instruments SN65DSI83 transceiver. The SN65DSI83 DSI to FlatLink bridge device features a single-channel MIPI D-PHY receiver front-end configuration with four lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI18 bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink-compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Single-Link LVDS with four data lanes per link. The SN65DSI83 device can support up to WUXGA1920 × 1200 at 60 frames per second, at 24 bpp with reduced blanking. The SN65DSI83 device is also suitable for applications using 60 fps 1366 × 768 /1280 × 800 at 18 bpp and 24 bpp. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces. Designed with industry-compliant interface technology, the SN65DSI83 device is compatible with a wide range of microprocessors, and is designed with a range of power management features including low-swing LVDS outputs, and the MIPI defined ultra-low power state (ULPS) support.

Main features:

- LVDS Output Clock Range of 25 MHz to 154MHz.
- Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking

- ESD Rating ±2 kV

## 4.8 LED

The i.MX8M-CM features a green LED controlled by GPIO4_IO28 signal of the i.MX8M. The LED is ON when GPIO4_IO28 is logic Low.

# 5. SODIMM204 connector

The i.MX8M-CM exposes a 204 pin SO-DIMM connector.

Recommended mating Connector socket for custom board interfacing are the following connectors (or equivalent):

- TE Connectivity 2013289-2 or 2013289-1
- Cvilux CS69-2042CA0-R0
- JAE MM80-204B1-1

| SODIMM Pin | Signal | i.MX8M Ball | Alt-0 | Alt-1 | Alt-2 | Alt-3 | Alt-4 | Alt-5 |
|---|---|---|---|---|---|---|---|---|
| 1 | ETH1_TX1_P | | | | | | | |
| 3 | ETH1_TX1_N | | | | | | | |
| 5 | ETH1_RX1_P | | | | | | | |
| 7 | ETH1_RX1_N | | | | | | | |
| 9 | ETH1_TX2_P | | | | | | | |
| 11 | ETH1_TX2_N | | | | | | | |
| 13 | ETH1_RX2_P | | | | | | | |
| 15 | ETH1_RX2_N | | | | | | | |
| 17 | ETH1_LED_ACT | | | | | | | |
| 19 | ETH1_LED_LINK100 | | | | | | | |
| 21 | SD2_nCD | L21 | usdhc2.CD_B | | | | | gpio2.IO[12] |
| 23 | ETH1_LED_LINK1000 | | | | | | | |
| 25 | GPIO3_IO14 | M20 | rawnand.DQS | qspi.B_DATA[3] | | | | gpio3.IO[14] |
| 27 | GPIO3_IO12 | L19 | rawnand.DATA06 | qspi.B_DATA[1] | | | | gpio3.IO[12] |
| 29 | CN_PCIE1_REF_CLK_P | K25 | | | | | | |
| 31 | CN_PCIE1_REF_CLK_N | K24 | | | | | | |
| 33 | CN_PCIE1_TX_P | J25 | | | | | | |
| 35 | CN_PCIE1_TX_N | J24 | | | | | | |
| 37 | CN_PCIE1_RX_P | H25 | | | | | | |
| 39 | CN_PCIE1_RX_N | H24 | | | | | | |
| 41 | PCIE2_REF_CLK_N | F24 | | | | | | |
| 43 | PCIE2_REF_CLK_P | F25 | | | | | | |
| 45 | PCIE2_TX_N | E24 | | | | | | |
| 47 | PCIE2_TX_P | E25 | | | | | | |
| 49 | PCIE2_RX_N | D24 | | | | | | |
| 51 | PCIE2_RX_P | D25 | | | | | | |
| 53 | CSI1_D0_P | B23 | | | | | | |
| 55 | CSI1_D0_N | A23 | | | | | | |
| 57 | CSI1_CLK_P | B22 | | | | | | |
| 59 | CSI1_CLK_N | A22 | | | | | | |
| 61 | CSI2_D2_P | B21 | | | | | | |
| 63 | CSI2_D2_N | A21 | | | | | | |
| 65 | CSI2_D1_P | B20 | | | | | | |
| 67 | CSI2_D1_N | A20 | | | | | | |
| 69 | CSI2_CLK_P | B19 | | | | | | |
| 71 | CSI2_CLK_N | A19 | | | | | | |
| 73 | USB1_VBUS | D14 | | | | | | |
| 75 | USB1_ID | C14 | | | | | | |
| 77 | USB1_D_P | A14 | | | | | | |
| 79 | USB1_D_N | B14 | | | | | | |
| 81 | USB1_TX_P | A13 | | | | | | |
| 83 | USB1_TX_N | B13 | | | | | | |
| 85 | USB1_RX_P | A12 | | | | | | |
| 87 | USB1_RX_N | B12 | | | | | | |
| 89 | USB2_D_P | A10 | | | | | | |
| 91 | USB2_D_N | B10 | | | | | | |
| 93 | USB2_TX_P | A9 | | | | | | |
| 95 | USB2_TX_N | B9 | | | | | | |
| 97 | USB2_RX_P | A8 | | | | | | |
| 99 | USB2_RX_N | B8 | | | | | | |
| 101 | USB2_VBUS | D9 | | | | | | |
| 103 | USB2_ID | C9 | | | | | | |
| 105 | PCIE2_nCLKREQ | F9 | i2c4.SDA | pwm1.OUT | | | | gpio5.IO[21] |
| 107 | UART1_TXD | A7 | uart1.TX | ecspi3.MOSI | | | | gpio5.IO[23] |
| 109 | UART3_TXD | B7 | uart3.TX | uart1.RTS_B | | | | gpio5.IO[27] |
| 111 | UART3_RXD | A6 | uart3.RX | uart1.CTS_B | | | | gpio5.IO[26] |
| 113 | UART2_RXD | B6 | uart2.RX | ecspi3.MISO | | | | gpio5.IO[24] |
| 115 | ECSPI2_SS0 | A5 | ecspi2.SS0 | uart4.RTS_B | | | | gpio5.IO[13] |
| 117 | ECSPI2_MISO | B5 | ecspi2.MISO | uart4.CTS_B | | | | gpio5.IO[12] |
| 119 | ECSPI1_MOSI | A4 | ecspi1.MOSI | uart3.TX | | | | gpio5.IO[7] |
| 121 | UART3_CTS | B4 | ecspi1.MISO | uart3.CTS_B | | | | gpio5.IO[8] |
| 123 | SAI1_MCLK | A3 | sai1.MCLK | sai5.MCLK | | | | gpio4.IO[20] |
| 125 | SAI1_TXD6 | B3 | sai1.TX_DATA[6] | sai6.RX_SYNC | | | coresight.TRACE[15] | gpio4.IO[18] |
| 127 | SAI1_TXD2 | B2 | sai1.TX_DATA[2] | sai5.TX_DATA[2] | | | coresight.TRACE[11] | gpio4.IO[14] |
| 129 | SAI1_TXD5 | C2 | sai1.TX_DATA[5] | sai6.RX_DATA[0] | sai6.TX_SYNC | | coresight.TRACE[14] | gpio4.IO[17] |
| 131 | SAI1_TXD7 | C1 | sai1.TX_DATA[7] | sai6.MCLK | sai1.TX_BCLK | | | gpio4.IO[19] |
| 133 | SAI1_TXD4 | D2 | sai1.TX_DATA[4] | sai6.RX_BCLK | sai6.TX_DATA[0] | | coresight.TRACE[13] | gpio4.IO[16] |
| 135 | SAI1_TXD3 | D1 | sai1.TX_DATA[3] | sai5.TX_DATA[3] | sai6.TX_BCLK | | coresight.TRACE[12] | gpio4.IO[15] |
| 137 | SAI1_TXD1 | E2 | sai1.TX_DATA[1] | sai5.TX_DATA[1] | | | coresight.TRACE[10] | gpio4.IO[13] |
| 139 | SAI1_TXC | E1 | sai1.TX_BCLK | sai5.TX_BCLK | | | coresight.TRACE[8] | gpio4.IO[11] |
| 141 | SAI1_TXD0 | F2 | sai1.TX_DATA[0] | sai5.TX_DATA[0] | | | coresight.TRACE[9] | gpio4.IO[12] |
| 143 | SAI1_RXD5 | F1 | sai1.RX_DATA[5] | sai6.TX_DATA[0] | sai6.RX_SYNC | | coresight.TRACE[6] | gpio4.IO[7] |
| 145 | SAI1_RXD6 | G2 | sai1.RX_DATA[6] | sai6.TX_SYNC | sai1.TX_SYNC | sai1.TX_DATA[4] | coresight.TRACE[7] | gpio4.IO[8] |
| 147 | SAI1_RXD7 | G1 | sai1.RX_DATA[7] | sai6.MCLK | | | coresight.EVENTO | gpio4.IO[9] |
| 149 | SAI1_RXD2 | H2 | sai1.RX_DATA[2] | sai5.RX_DATA[2] | | | coresight.TRACE[3] | gpio4.IO[4] |
| 151 | SAI1_TXFS | H1 | sai1.TX_SYNC | sai5.TX_SYNC | | | coresight.EVENTI | gpio4.IO[10] |
| 153 | SAI1_RXD3 | J2 | sai1.RX_DATA[3] | sai5.RX_DATA[3] | sai6.RX_BCLK | | coresight.TRACE[4] | gpio4.IO[5] |
| 155 | SAI1_RXD4 | J1 | sai1.RX_DATA[4] | sai6.TX_BCLK | sai6.RX_DATA[0] | sai1.RX_SYNC | coresight.TRACE[5] | gpio4.IO[6] |
| 157 | SAI1_RXD0 | K2 | sai1.RX_DATA[0] | sai5.RX_DATA[0] | | | coresight.TRACE[1] | gpio4.IO[2] |
| 159 | SAI1_RXC | K1 | sai1.RX_BCLK | sai5.RX_BCLK | | | coresight.TRACE[0] | gpio4.IO[1] |
| 161 | SAI1_RXD1 | L2 | sai5.RX_DATA[1] | sai1.TX_DATA[3] | sai1.TX_SYNC | sai5.TX_BCLK | | gpio3.IO[22] |
| 163 | SAI1_RXFS | L1 | sai5.RX_SYNC | sai1.TX_DATA[0] | | | | gpio3.IO[19] |
| 165 | MIC | | | | | | | |
| 167 | GND | | | | | | | |
| 169 | UART1_RXD | C7 | uart1.RX | ecspi3.SCLK | | | | gpio5.IO[22] |
| 171 | UART2_TXD | D6 | uart2.TX | ecspi3.SS0 | | | | gpio5.IO[25] |
| 173 | ECSPI1_SCLK | D5 | ecspi1.SCLK | uart3.RX | | | | gpio5.IO[6] |
| 175 | ECSPI2_SCLK | C5 | ecspi2.SCLK | uart4.RX | | | | gpio5.IO[10] |
| 177 | ECSPI2_MOSI | E5 | ecspi2.MOSI | uart4.TX | | | | gpio5.IO[11] |
| 179 | UART3_RTS | D4 | ecspi1.SS0 | uart3.RTS_B | | | | gpio5.IO[9] |
| 181 | UART4_RXD | C6 | uart4.RX | uart2.CTS_B | pcie1.CLKREQ_B | | | gpio5.IO[28] |
| 183 | UART4_TXD | B7 | uart4.TX | uart2.RTS_B | pcie2.CLKREQ_B | | | gpio5.IO[29] |
| 185 | SYS_nRST | | | | | | | |
| 187 | NVCC_3V3 | | | | | | | |
| 189 | NVCC_3V3 | | | | | | | |
| 191 | VIN_4V2 | | | | | | | |
| 193 | VIN_4V2 | | | | | | | |
| 195 | VIN_4V2 | | | | | | | |
| 197 | VIN_4V2 | | | | | | | |
| 199 | VIN_4V2 | | | | | | | |
| 201 | GND | | | | | | | |
| 203 | GND | | | | | | | |

| SODIMM Pin | Signal | i.MX8M Ball | Alt-0 | Alt-1 | Alt-2 | Alt-3 | Alt-4 | Alt-5 |
|---|---|---|---|---|---|---|---|---|
| 2 | GND | | | | | | | |
| 4 | MX8_ONOFF | W21 | | | | | | |
| 6 | USB1_SS_SEL | K19 | rawnand.RE_B | qspi.A_DQS | | | | gpio3.IO[15] |
| 8 | BOOT_MODE1 | V6 | | | | | | |
| 10 | BOOT_MODE0 | W6 | | | | | | |
| 12 | PCIe_nRST | J22 | rawnand.DATA05 | qspi.B_DATA[0] | | | | gpio3.IO[11] |
| 14 | TCPC_nINT | F21 | rawnand.CE2_B | qspi.A_SS1_B | | | | gpio3.IO[3] |
| 16 | GPIO1_IO05 | P7 | gpio1.IO[5] | m4.NMI | | | | ccmsrcgpcmix.PMIC_READY |
| 18 | SD2_nRST | R22 | usdhc2.RESET_B | | | | | gpio2.IO[19] |
| 20 | SD2_DATA2 | P22 | usdhc2.DATA2 | | | | | gpio2.IO[17] |
| 22 | GND | | | | | | | |
| 24 | SD2_DATA1 | N21 | usdhc2.DATA1 | | | | | gpio2.IO[16] |
| 26 | SD2_DATA0 | N22 | usdhc2.DATA0 | | | | | gpio2.IO[15] |
| 28 | SD2_DATA3 | P21 | usdhc2.DATA3 | | | | | gpio2.IO[18] |
| 30 | SD2_WP | M21 | usdhc2.WP | | | | | gpio2.IO[20] |
| 32 | SD2_CMD | M22 | usdhc2.CMD | | | | | gpio2.IO[14] |
| 34 | SD2_CLK | L22 | usdhc2.CLK | | | | | gpio2.IO[13] |
| 36 | GPIO3_IO2 | G21 | rawnand.CE1_B | qspi.A_SS0_B | | | | gpio3.IO[2] |
| 38 | BT_USB_D_N | | | | | | | |
| 40 | BT_USB_D_P | | | | | | | |
| 42 | CLKO2 | J6 | gpio1.IO[15] | usb2.OTG_OC | | | | pwm4.OUT |
| 44 | GND | | | | | | | |
| 46 | GPIO1_IO12 | L7 | gpio1.IO[12] | usb1.OTG_PWR | | | | sdma2.EXT_EVENT[1] |
| 48 | SPDIF_TX | F6 | spdif1.OUT | pwm3.OUT | | | | gpio5.IO[3] |
| 50 | SPDIF_RX | G6 | spdif1.IN | pwm2.OUT | | | | gpio5.IO[4] |
| 52 | CSI1_D2_N | C23 | | | | | | |
| 54 | CSI1_D2_P | B24 | | | | | | |
| 56 | CSI1_D1_P | D22 | | | | | | |
| 58 | CSI1_D1_N | C22 | | | | | | |
| 60 | CSI1_D3_P | D21 | | | | | | |
| 62 | CSI1_D3_N | C21 | | | | | | |
| 64 | CSI2_D0_P | D20 | | | | | | |
| 66 | CSI2_D0_N | C20 | | | | | | |
| 68 | CSI2_D3_P | D19 | | | | | | |
| 70 | CSI2_D3_N | C19 | | | | | | |
| 72 | GND | | | | | | | |
| 74 | GPIO1_IO13 | K6 | gpio1.IO[13] | usb1.OTG_OC | | | | pwm2.OUT |
| 76 | SAI5_MCLK | K4 | sai5.MCLK | sai1.TX_BCLK | | | coresight.TRACE_CLK | gpio3.IO[25] |
| 78 | SAI5_RXD3 | K5 | sai5.RX_DATA[3] | sai1.TX_DATA[5] | sai4.MCLK | | | gpio3.IO[24] |
| 80 | SAI5_RXD1 | L4 | sai5.RX_DATA[1] | sai1.TX_DATA[3] | sai1.TX_SYNC | sai5.TX_BCLK | | gpio3.IO[22] |
| 82 | SAI5_RXC | L5 | sai5.RX_BCLK | sai1.TX_DATA[1] | | | | gpio3.IO[20] |
| 84 | I2C1_SDA | E8 | i2c1.SDA | enet1.MDIO | | | | gpio5.IO[15] |
| 86 | I2C1_SCL | E7 | i2c2.SCL | enet1.1588_EVENT1_IN | | | | gpio5.IO[16] |
| 88 | I2C3_SDA | E9 | i2c3.SDA | pwm3.OUT | pcie1.CLKREQ_B | | | gpio5.IO[19] |
| 90 | SPDIF_EXT_CLK | E6 | spdif1.EXT_CLK | pwm1.OUT | | | | gpio5.IO[5] |
| 92 | PCIE1_nCLKREQ | F8 | i2c4.SCL | pwm2.OUT | pcie2.CLKREQ_B | | | gpio5.IO[20] |
| 94 | I2C3_SCL | G8 | i2c3.SCL | pwm4.OUT | gpt3.CLK | | | gpio5.IO[18] |
| 96 | GND | | | | | | | |
| 98 | SAI5_RXD2 | M4 | sai5.RX_DATA[2] | sai1.TX_DATA[4] | sai1.TX_SYNC | sai5.TX_DATA[0] | | gpio3.IO[23] |
| 100 | SAI5_RXD0 | M5 | sai5.RX_DATA[0] | sai1.TX_DATA[2] | sai1.TX_SYNC | sai5.TX_SYNC | | gpio3.IO[21] |
| 102 | GPIO1_IO08 | N7 | gpio1.IO[8] | enet1.1588_EVENT0_IN | | | | usdhc2.RESET_B |
| 104 | SAI5_RXFS | N4 | sai5.RX_SYNC | sai1.TX_DATA[0] | | | | gpio3.IO[19] |
| 106 | HDMI_DDC_SCL | R3 | | | | | | |
| 108 | HDMI_DDC_SDA | P3 | | | | | | |
| 110 | HDMI_HPD | W2 | | | | | | |
| 112 | HDMI_CEC | W3 | | | | | | |
| 114 | HDMI_AUX_N | V2 | | | | | | |
| 116 | HDMI_AUX_P | V1 | | | | | | |
| 118 | HDMI_TX0_N | T2 | | | | | | |
| 120 | HDMI_TX0_P | T1 | | | | | | |
| 122 | HDMI_CLK_N | R1 | | | | | | |
| 124 | HDMI_CLK_P | R2 | | | | | | |
| 126 | HDMI_TX2_N | N1 | | | | | | |
| 128 | HDMI_TX2_P | N2 | | | | | | |
| 130 | HDMI_TX1_N | U1 | | | | | | |
| 132 | HDMI_TX1_P | U2 | | | | | | |
| 134 | GND | | | | | | | |
| 136 | LVDS0_TX0_N | | | | | | | |
| 138 | LVDS0_TX0_P | | | | | | | |
| 140 | LVDS0_TX1_N | | | | | | | |
| 142 | LVDS0_TX1_P | | | | | | | |
| 144 | LVDS0_TX2_N | | | | | | | |
| 146 | LVDS0_TX2_P | | | | | | | |
| 148 | LVDS0_CLK_N | | | | | | | |
| 150 | LVDS0_CLK_P | | | | | | | |
| 152 | LVDS0_TX3_N | | | | | | | |
| 154 | LVDS0_TX3_P | | | | | | | |
| 156 | SAI2_RXC | H3 | sai2.RX_BCLK | sai5.TX_BCLK | | | | gpio4.IO[22] |
| 158 | HEADPHONE_R | | | | | | | |
| 160 | HEADPHONE_L | | | | | | | |
| 162 | SAI2_MCLK | H5 | sai2.MCLK | sai5.MCLK | sai5.RX_SYNC | | | gpio4.IO[27] |
| 164 | SPK_RP | | | | | | | |
| 166 | SPK_RN | | | | | | | |
| 168 | GND | | | | | | | |
| 170 | JTAG_TCK | T5 | | | | | | |
| 172 | JTAG_TMS | V5 | | | | | | |
| 174 | JTAG_TRST_B | U6 | | | | | | |
| 176 | JTAG_TDO | U5 | | | | | | |
| 178 | JTAG_TDI | W5 | | | | | | |
| 180 | GPIO1_IO01 | T7 | | | | | | |
| 182 | GPIO1_IO03 | P4 | | | | | | |
| 184 | CSI_nRST | N5 | gpio1.IO[9] | enet1.1588_EVENT0_OUT | | | | sdma2.EXT_EVENT[0] |
| 186 | GPIO5_IO2 | D3 | sai3.MCLK | pwm4.OUT | | | | gpio5.IO[2] |
| 188 | NVCC_3V3 | | | | | | | |
| 190 | NVCC_3V3 | | | | | | | |
| 192 | VIN_4V2 | | | | | | | |
| 194 | VIN_4V2 | | | | | | | |
| 196 | VIN_4V2 | | | | | | | |
| 198 | VIN_4V2 | | | | | | | |
| 200 | VIN_4V2 | | | | | | | |
| 202 | GND | | | | | | | |
| 204 | GND | | | | | | | |

# 6. CPU Module interfaces

## 6.1 Display interfaces

i.MX8M-CM provides the following display interfaces:

- HDMI

  i.MX8M-CM HDMI 2.0 interface is derived from the i.MX8M HD Display Transmitter Controller IP. The controller supports the following protocols:

  - HDMI1.4, HDMI 2.0a support for resolution up to 4096x2160p60
  - HDCP 2.2 and HDCP 1.4
  - Pixel clock up to 596 MHz
  - Display Port 1.3
  - All standards share the same pins

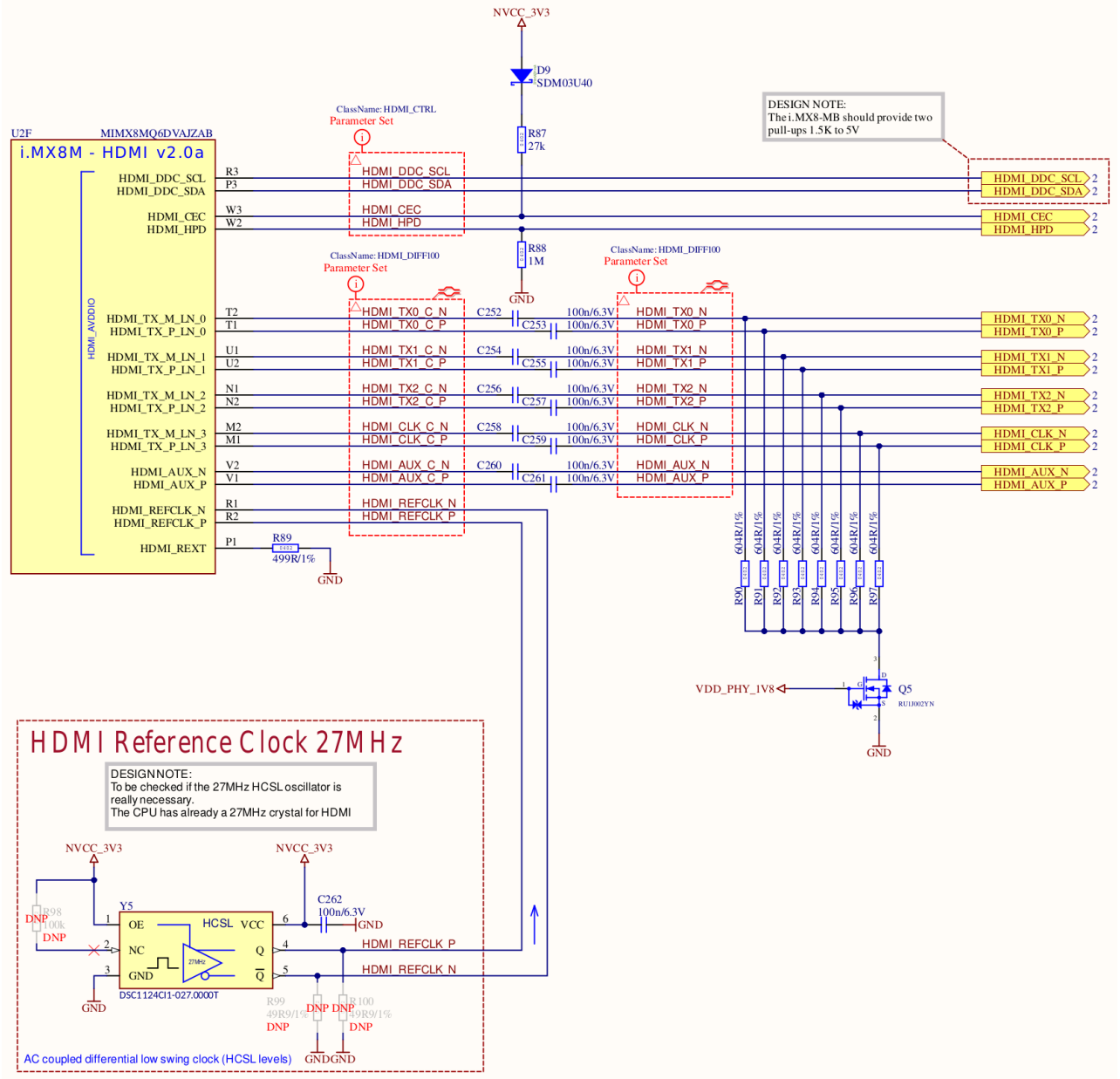



*Figure 6.1:*

- MIPI DSI

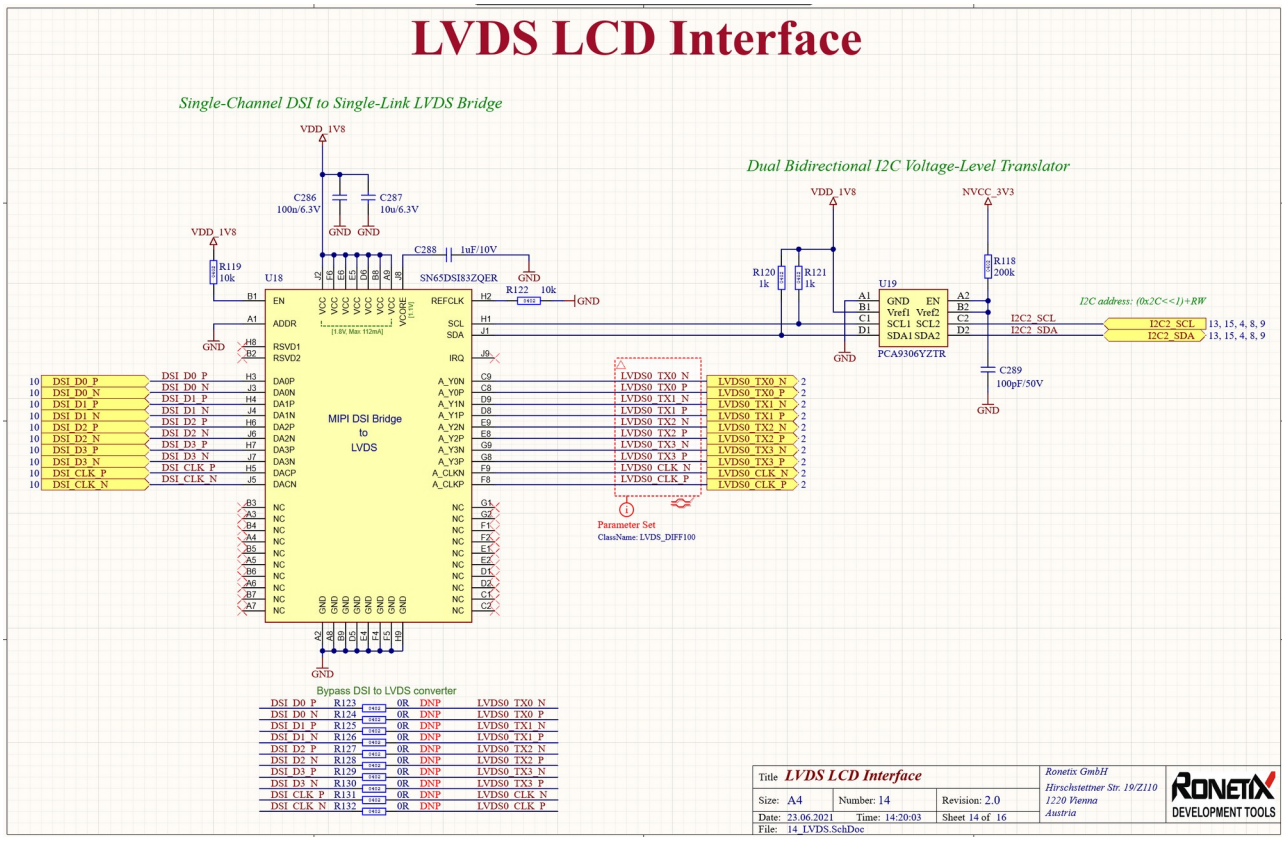
  The MIPI-DSI interface is based on the four-lane MIPI display interface available with the iMX8M SoC. The DSI signals are available on the SODIMM204 connector if the SN65DSI83 is not assembled.

  The following main features are supported:

  - Up to 4 data lanes support D-PHY

- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)
- Supports High Speed and Low Power operation
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

- LVDS Interface (optional) – using Texas Instruments SN65DSI83 MIPI-DSI to LVDS bridge. If not assembled, then all DSI signals are available on the SODIMM204 connector. Texas Instruments SN65DSI83 supports following main features:
  - LVDS Output Clock Range of 25 MHz to 154MHz.
  - Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
  - Capable of supporting the full resolution of the iMX8M MIPI-DSI interface with reduced blanking
  - ESD Rating ±2 kV




## 6.2 MIPI-CSI Camera interface

i.MX8M-CM MIPI-CSI interface is derived from the four-lane MIPI CSI1 host controller (MIPI_CSI1) integrated into the iMX8M SoC. The CSI1 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-1 specification, providing an interface between CL-SOM-iMX8 and a MIPI CSI-1 compliant camera sensor. The following main features are supported:

- Up-to four data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Supports unidirectional Master operation
- Supports high speed mode (80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Support 5M pixel at 15 fps, 1080p30, 720p60, VGA at 60 fps

- Support for all CSI-2 data types:
  - RGB444, RGB555, RGB565, RGB666, RGB888
  - Legacy YUV420 8 bit
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - User Defined Data Types

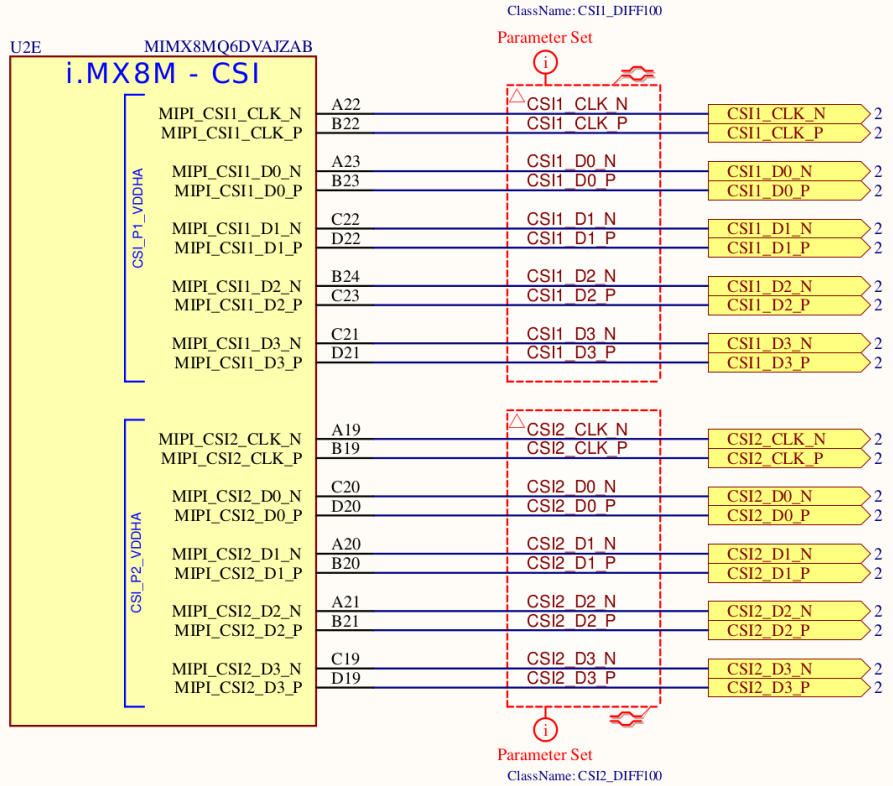



*Figure 6.2: MIPI-CSI*

Please refer to the i.MX8M Reference manual for additional details.

## 6.3 USB interface

The iMX8M SoC is equipped two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains USB 3.0 core, which can operate in both 3.0 and 2.0 mode. One port supports dual-role functionality, while the second port is configured permanently for host mode. USB ports support the following main features:

- Complies with USB specification rev 3.0 (xHCI compatible)
- Can operate in both 3.0 and 2.0 mode
- 32 endpoints per slot

- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low speed (1.5 Mbit/s) operations.
- Super-speed operation is not supported when OTG is enabled

Please refer to the i.MX8M Reference manual for additional details.

## 6.4 PCI-Express

The i.MX8M SoC is equipped with two single lane PCI Express port (PCIe) v2.1 ports.

On i.MX8M-CM SoM PCIe-1 is connected to the WiFi Module, but optionally can be routed to the SODIMM204 connector. PCIe-2 is available on the SODIMM204 connector and requires an external PCIe clock.

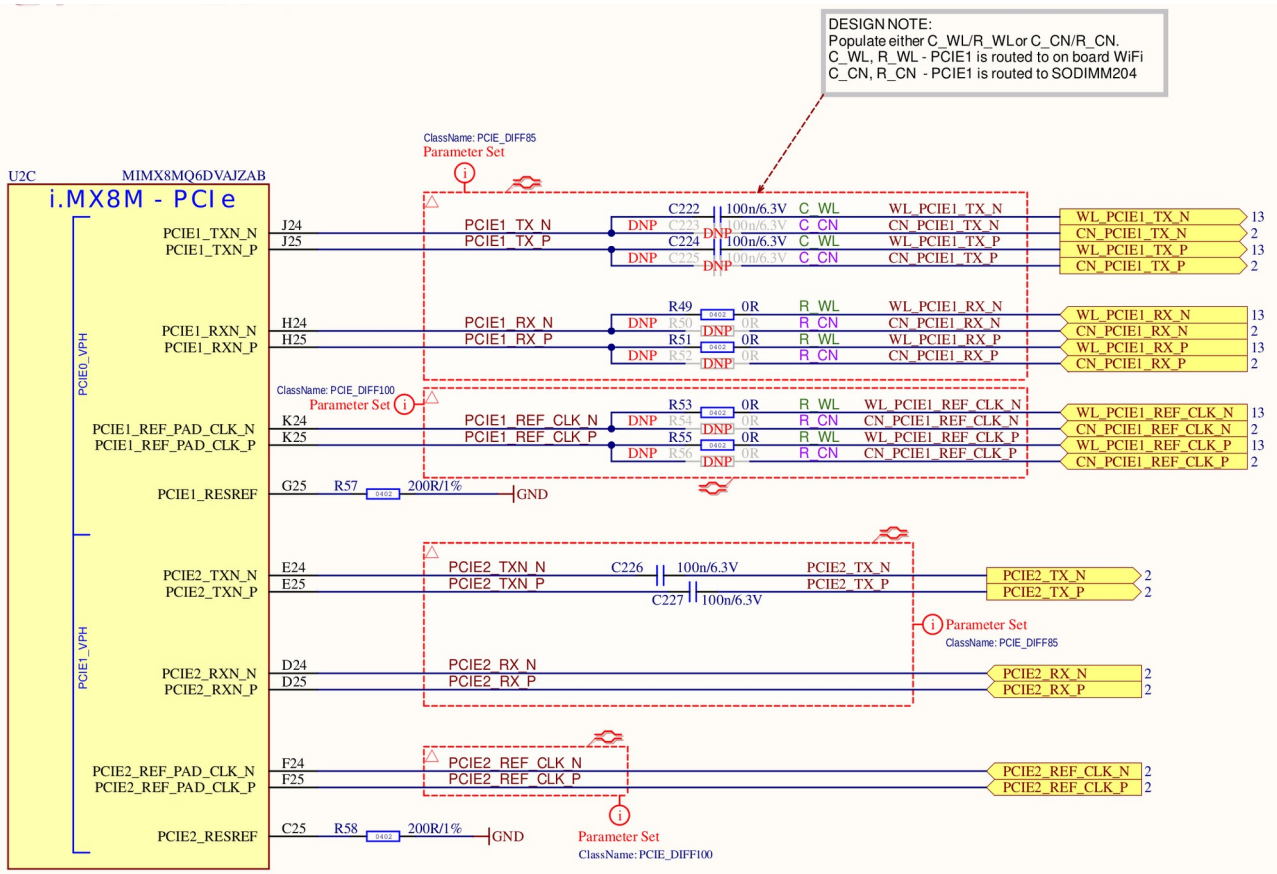



*Figure 6.3: PCIe*

The PCI Express ports support the following main features:

- Single lane compliant with PCI Express base specification v2.1 (6.0Gbps)

- Dual mode operation to function as root complex or endpoint
- Port solution includes the controller, an analog PHY macro, and application logic to source and sink data

Please refer to the i.MX8M Reference manual for additional details.

## 6.5 MMC, SD, SDIO

The i.MX8M SoC is equipped with two MMC/SD/SDIO controller IPs (uSDHC). On i.MX8M-CM SD1 is connected to the eMMC. SD2 is available on the SODIMM204 connector.

The uSDHC supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- Dedicated “card detection” and “write protection” signals
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

Please refer to the i.MX8M Reference manual for additional details.

## 6.6 UART

The i.MX8M-CM exposes up to 4 UART interfaces some of which are multiplexed with other peripherals.

The i.MX8M UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.

- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

Please refer to the i.MX8M Reference manual for additional details.

## 6.7 I2C

The i.MX8M SoC is equipped with three I2C bus interfaces. I2C1 and I2C3 are available on the SODIMM204 connector. I2C2 is used internally, not available on SODIMM204. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

I2C usage table:

I2C USAGE AND ADDRESS TABLE

| NAME | PERIPHERAL | ADDRESS |
|---|---|---|
| I2C1 | i.MX8-MB: USB3.0 Power Switch | (0x050<<1)+RW |
| | i.MX8-MB: RTC clock | (0x051<<1)+RW |
| | i.MX8-MB: miniPCIEe Ref. Clock | (0x6A<<1)+RW |
| | i.MX8-MB: Camera on CSI1 | (0x3C<<1)+RW |
| I2C2 only on CM | i.MX8-CM: PMIC control | (0x4B<<1)+RW |
| | i.MX8-CM: WiFi Ref. Clock | (0x68<<1)+RW |
| | i.MX8-CM: EEPROM | (0x50<<1)+RW |
| | i.MX8-CM: Audio Codec | (0x1A<<1)+RW |
| | i.MX8-CM: LVDS | (0x2C<<1)+RW |
| I2C3 | i.MX8-MB: mPCIe connector | |
| | i.MX8-MB: Camera on CSI2 | (0x3C<<1)+RW |
| | | |
| | | |

*Figure 6.4: I2C usage*

## 6.8 SPI

Up-to three SPI interfaces are accessible through the i.MX8M-CM base board interface. The SPI interfaces are derived from i.MX8M integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX8M Reference manual for additional details.

## 6.9 Quad SPI

QSPI-A is connected onboard to a QSPI NOR Flash. QSPI.B is not available on SODIMM204.

The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX8M Reference manual for additional details.

## 6.10 PWM

Up to four PWM output signals are available at the i.MX8M-CM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

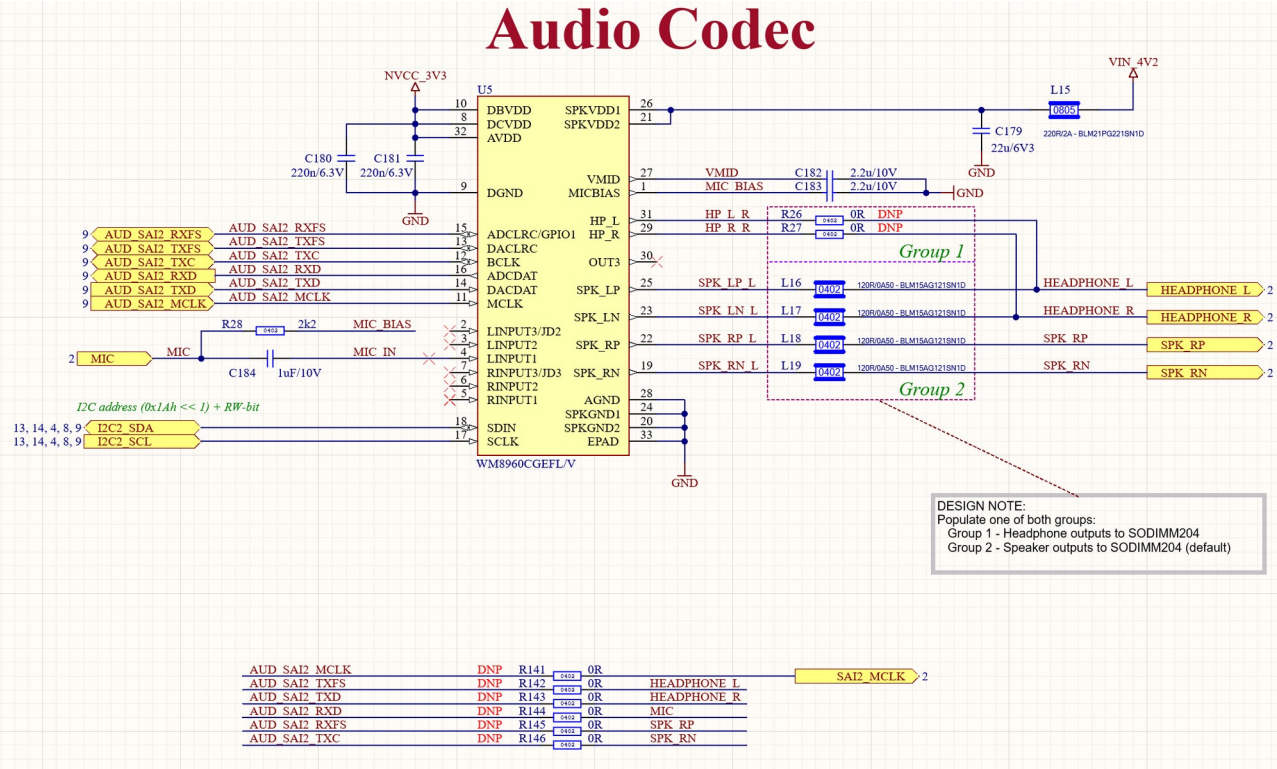
Please refer to the i.MX8M Reference manual for additional details.

## 6.11 Analog Audio

i.MX8M-CM analog audio functionality is implemented by the Wolfson WM8960 audio code. WM8960 is connected to I.MX8M SAI2 port.

Please refer to the WM8960 datasheet for additional details.

If the WM8960 is not populated, the SAI signals can be bypassed to the SODIMM204 connector. Either the speaker or the headphone signals can be provided to the SODIMM204 connector.



## 6.12 GPIO

Up-to 7 of the i.MX8M general purpose input/output (GPIO) signals are available on the SODIMM204 connector. When configured as an output, it is possible to write to an i.MX8M register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M register. In addition GPIOs peripheral can produce interrupts.

## 6.13 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the SODIMM204 connector.

# 7. Power Supply

## 7.1 Power supply from base board

i.MX8M-CM is powered by regulated DC supply 3.8-5.0V

| Signal | Type | Description |
|---|---|---|
| VIN_4V2 | Power input | Main Power Supply 3.8-5.0V |
| GND | Power input | Common ground |

## 7.2 Power supply provided to base board

i.MX8M-CM provides a 3.3V power supply to the SODIMM204 connector.

| Signal | Type | Description |
|---|---|---|
| NVCC_3V3 | Power output | 3.3V, Max. 1.5A |

## 7.3 System Signals

| Signal | Type | Description |
|---|---|---|
| MX8_ONOFF | Input with Pull-Up resistor | ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF. |
| SYS_nRST | Input | PMIC Power On signal |

# 8. Electrical Specifications

## 8.1 Absolute maximum ratings

| Parameter | Mln | Max | Unit |
|---|---|---|---|
| VIN_4V2 – Main Power Supply | -0.3 | 5.25 | V |
| USB_VBUS - USB_HOST_VBUS, USB_OTG_VBUS | -0.3 | 5.25 | V |

## 8.2 Recommended Operating Conditions

| Parameter | Mln | Typ | Max | Unit |
|---|---|---|---|---|
| VIN_4V2 – Main Power Supply | 3.8 | 4.2 | 5.0 | V |
| VIN_4V2 – recommended source capability | | 4.0 | | A |

# 9. Operating Temperature Ranges

| Range | Temp. |
|---|---|
| Commercial | 0° to +70°C |
| Industrial | -40° to +85°C |

# 10. Cooling

A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the iMX8M-CM temperature specifications.

# 11. Mechanical Drawings

All dimensions are in millimeters.

The height of all parts is < 2mm.

The base board connector provides 2.8mm board to board clearance.

Board thickness is 1.0mm

## 11.1 Base board mounting

i.MX8M-CM SoM has two mounting holes for mounting to the base board which are plated and connected to GND.

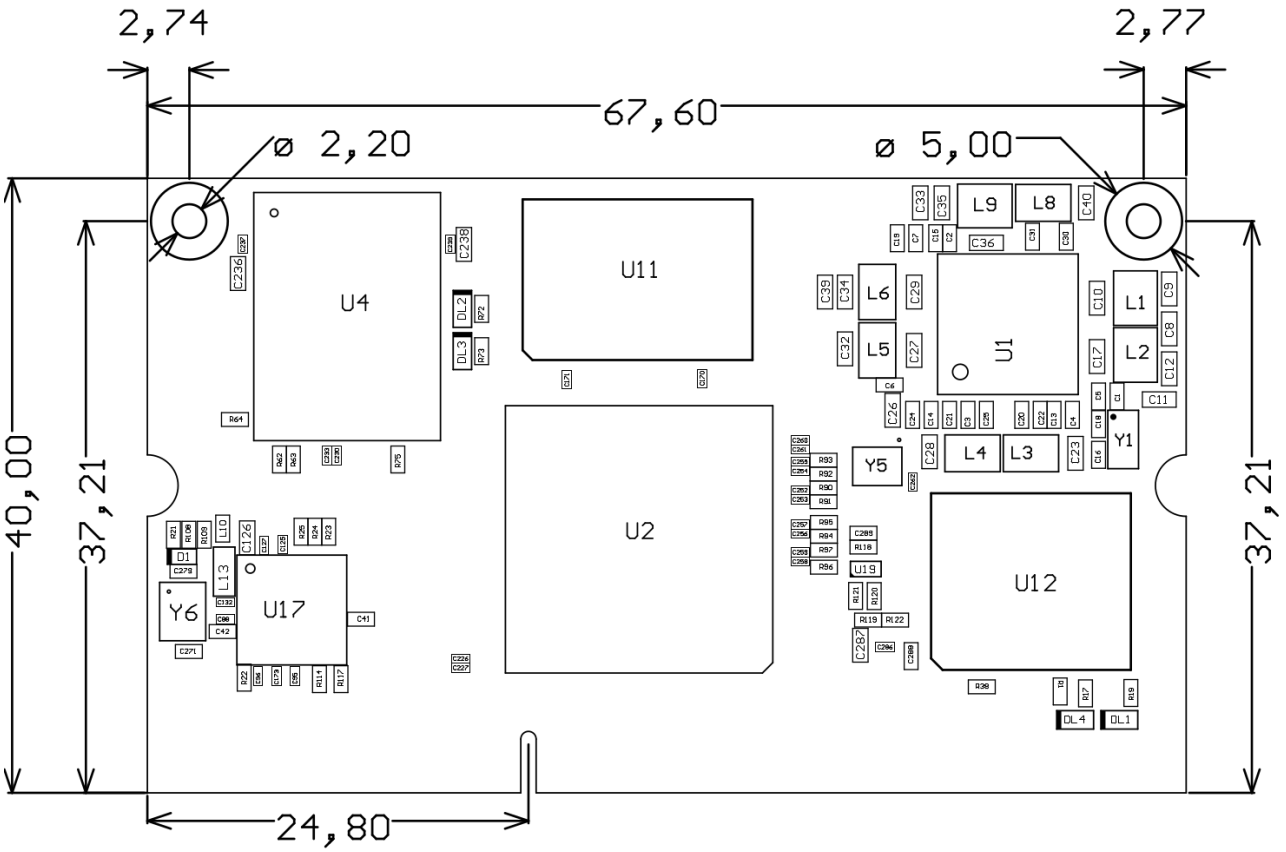



*Figure 11.1: Mechanical drawing*

## 11.2 Standoffs

Fix i.MX8M-CM to the base board by mounting two spacers with suitable screws. The spacers should be:

- M2x0.4, length 3.0mm

# 12. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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