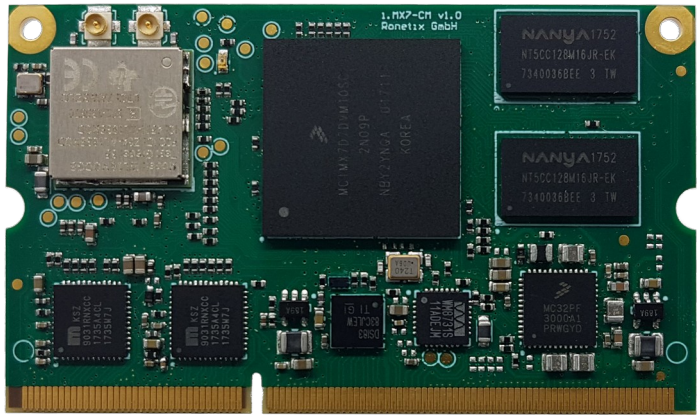
RONETIX
DEVELOPMENT TOOLS

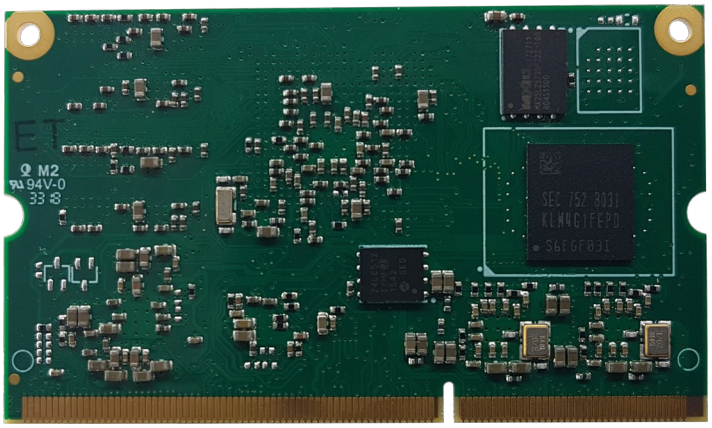
i.MX7-CM

CPU Module (SoM) with NXP i.MX7

Datasheet

rev 1.0





Ronetix Development Tools GmbH
Hirschstettner Str. 19/Z110
1220 Vienna
Austria
www.ronetix.at

1. Document Revision History

Revision	Date	Notes
1.0	10-Sep-2020	Initial release

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3. Overview

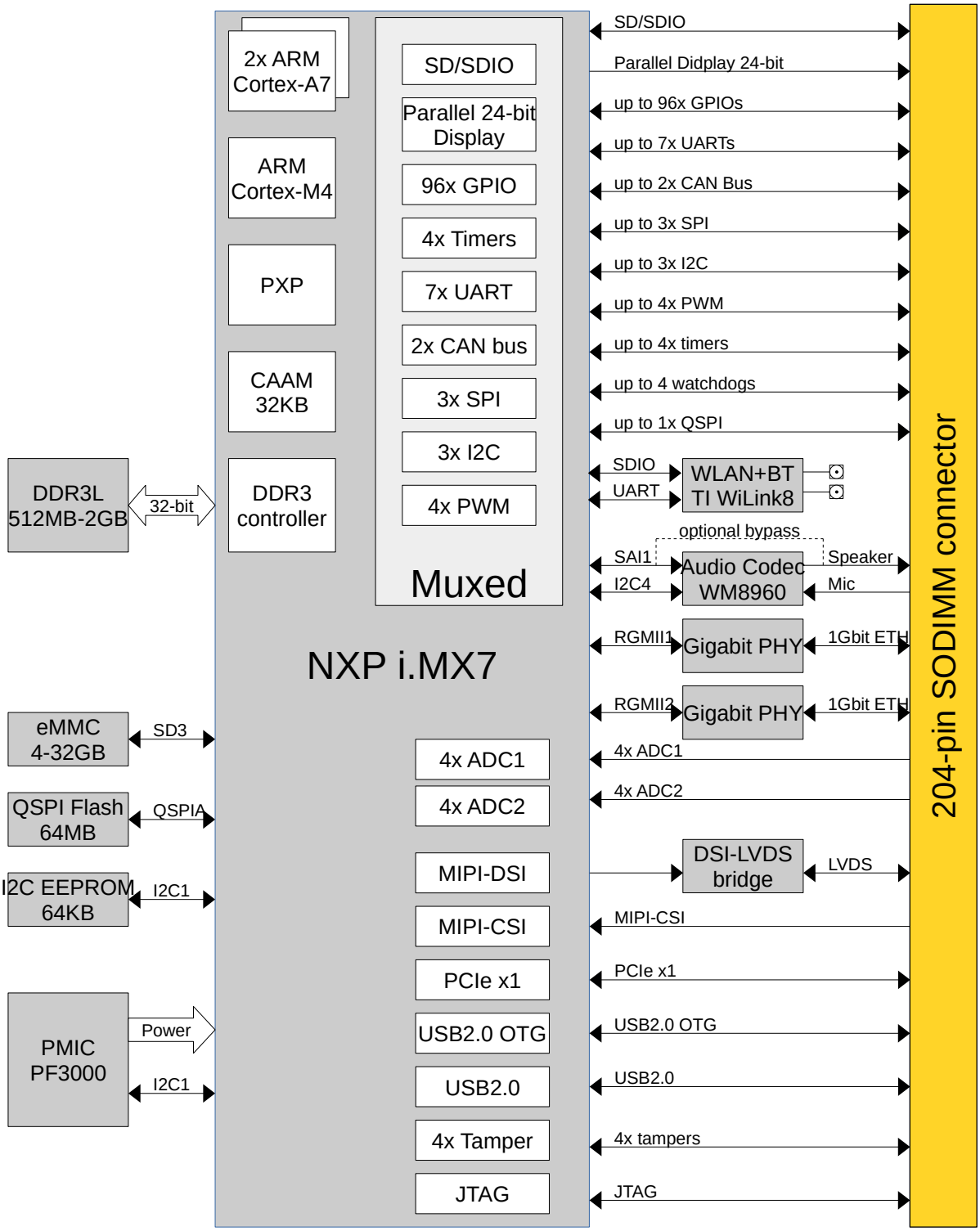
3.1 General Information

The **i.MX7-CM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX7 Dual family of multipurpose processors from which feature an ARM® Cortex™-A7 up to 1GHz + an additional ARM Cortex-M4. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A7 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

3.2 Highlights

CPU	• Dual ARM® Cortex™-A7 Core, 1GHz/800Mhz • ARM® Cortex™-M4, 200MHz
Memory	• RAM: 512MB DDR3L (optional up to 2 GiB) • eMMC: 4 GiB (optional: up to 32 GiB) • I2C EEPROM: 64KiB (optional) • QSPI NOR Flash: 64 MiB (optional)
Display	• LVDS, up to 1400 x 1050 @60Hz • Parallel 24-bit display interface, up to 1920 x 1080 @60Hz
Camera	• MIPI-CSI, 2 data lanes
Network	• Ethernet: 2x 10/100/1000Mbps • WiFi: WL1835MOD WiLink™ 8, 802.11b/g/n, single band combo 2×2 MIMO (optional) • Bluetooth: Bluetooth 4.2 Secure Connection Compliant (optional)
Audio	• Audio codec WM8960: Stereo Headphone, Stereo Class D Speaker 1W, Microphone
I/O	• PCIe x1 Gen. 2.1 • 1x USB2.0 OTG port • Up to 7x UART ports, up to 4 Mbps • Up to 2x CAN bus • 1x MMC/SD/SDIO • Up to 3x SPI • Up to 3x I2C • Up to 4x general purpose PWM signals • 8x general-purpose ADC channels • 4x tamper inputs • Up to 96x GPIO
Electrical	• Supply Voltage: 3.5 – 4.5V
Physical	• Board size: 67x40mm • SO-DIMM 200 JEDEC MO-274 module (67.6x40mm) • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90% • MTTF > 200000 hours

3.3 Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of i.MX7-CM SoM.

4.1 Power supply

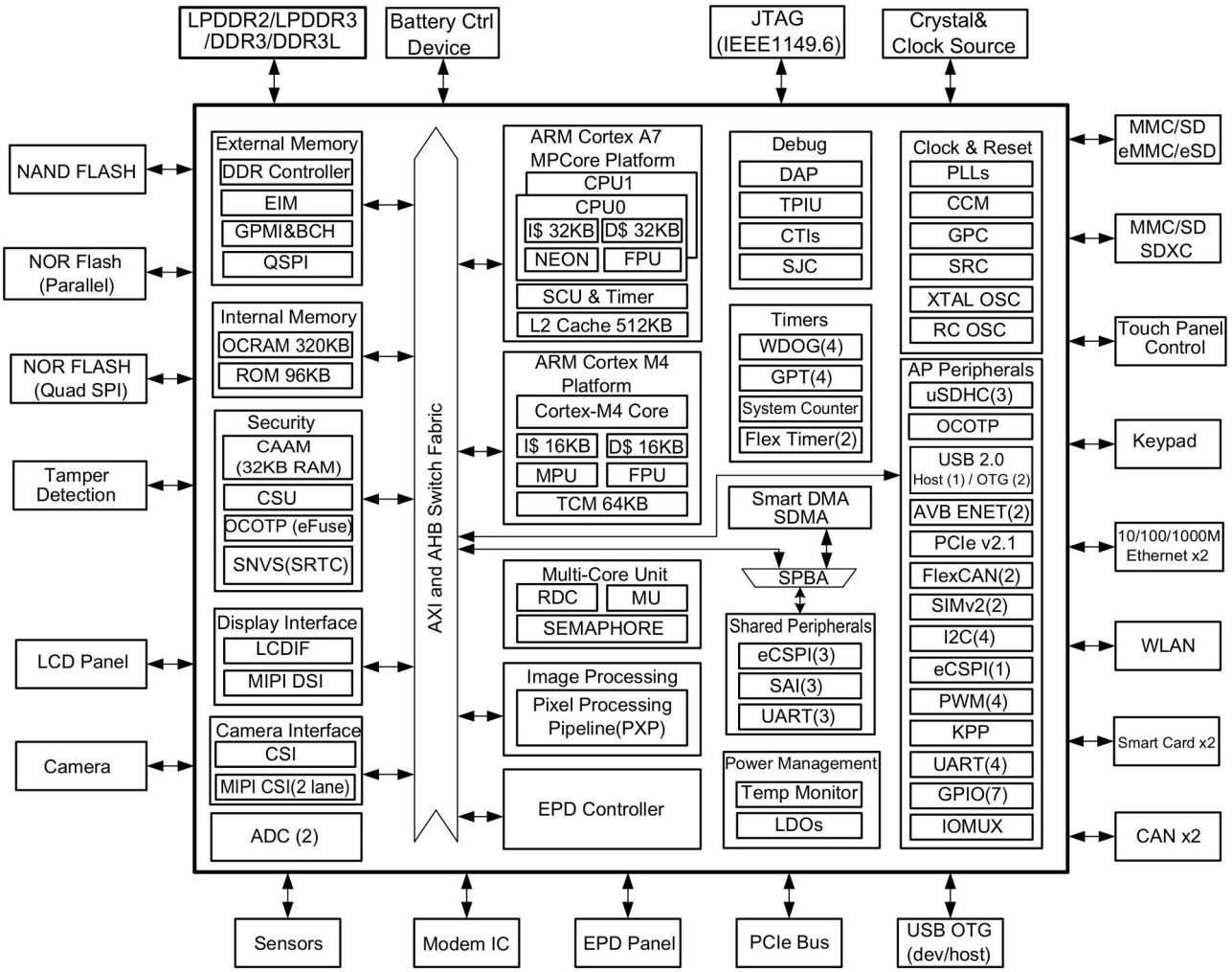
I.MX7-CM uses NXP's PF3000 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX7 series of application processors. The PMIC regulates all power rails required on CPU module from a single 3.5V-4.2V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU i.MX7D

The i.MX7Dual family of processors represents NXP's latest achievement in high-performance processing for low-power requirements with a high degree of functional integration. These processors are targeted towards the growing market of connected and portable devices. The i.MX7Dual family of processors features advanced implementation of the Arm® Cortex®-A7 core, which operates at speeds of up to 1 GHz and 1.2 GHz, depending on the part number. The i.MX7Dual family provides up to 32-bit DDR3/DDR3L/LPDDR2/LPDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

4.2.1 i.MX7D Block Diagram



4.2.2 CPU Platform

The i.MX7 Dual processor implements two ARM® Cortex®-A7 cores intended for high level O/S, with an ARM® Cortex®-M4 core dedicated for real-time tasks.

The ARM Cortex-A7 MPCore™ platform has the following features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology) Symmetric CPU
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache

  - Private Timer and Watchdog
  - NEON MPE (media processing engine) coprocessor
- The Arm Cortex-A7 Core complex shares:
  - General interrupt controller (GIC) with 128 interrupt support
  - Global timer
  - Snoop control unit (SCU)
  - 512 KB unified I/D L2 cache
  - Two master AXI bus interfaces output of L2 cache
  - Frequency of the core (including NEON and L1 cache), as per Table 9.
  - NEON MPE co-processor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline

The ARM Cortex-M4 platform includes the following features:

- Cortex-M4 CPU core operating at 200 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 64 KByte TCM (tightly-coupled memory)

4.3 Memory

4.3.1 DRAM

I.MX7-CM is standard equipped with 512 MB DDR3L memory. Optionally up to 2 GB can be assembled. The data bus is 32-bit wide and operates at 533 MHz.

4.3.2 eMMC – non-volatile storage memory

i.MX7-CM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.3.3 SPI NOR Flash

i.MX7-CM can be assembled with a QSPI NOR Flash.

The SPI Flash can be used as boot device.

4.3.4 I2C EEPROM

i.MX7-CM can be assembled with a I2C EEPROM.

4.4 Gigabit Ethernet

i.MX7-CM implements two full-featured 10/100/1000 Ethernet ports implemented with the two MACs built into the i.MX7 SoC, coupled with two KSZ9031 RGMII Ethernet PHYs from Micrel. Both Ethernet interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

4.5 WLAN

i.MX7-CM optional wireless communication is implemented with Texas Instrument WL1835MOD WLAN module.

WL1835MOD is a WiLink™ 8 Single-Band Combo Module enabling Wi-Fi®, Bluetooth® and Bluetooth® Low Energy(LE) functionality supports the following features:

- WLAN Baseband Processor and RF Transceiver Support of IEEE Std 802.11b, 802.11g, and 802.11n

- 20- and 40-MHz SISO and 20-MHz 2 × 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP)
- 2.4-GHz MRC Support for Extended Range
- Bluetooth 4.2 Secure Connection Compliant and CSA2 Support
- Dedicated Audio Processor Support of SBC Encoding + A2DP
- Dual-Mode Bluetooth and Bluetooth Low Energy

i.MX7-CM is equipped with two U.FL high frequency connectors for external antennas.

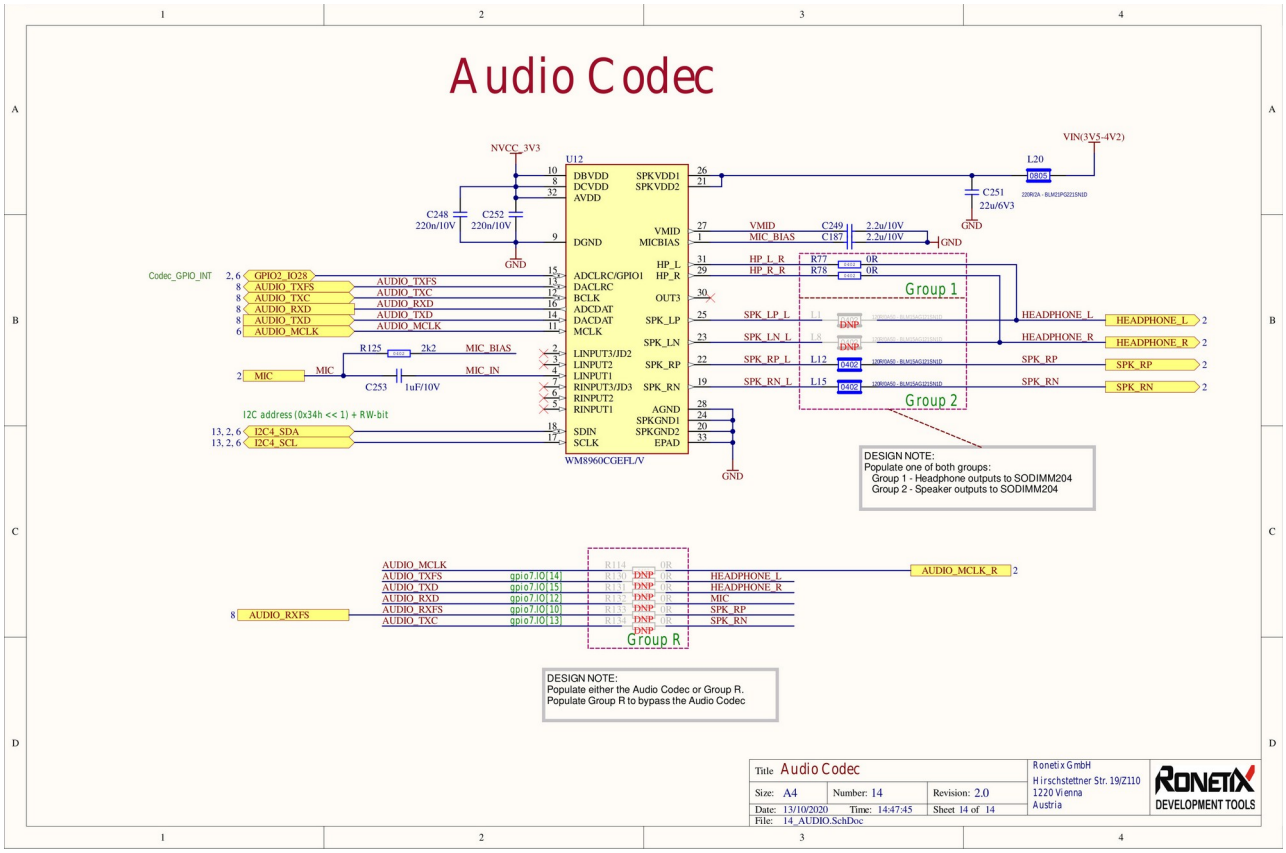
4.6 Audio

I.MX7-CM implements an audio codec WM8960 (assembled optional) . The WM8960 supports the following features:

- Stereo class D speaker driver, 1W per channel
- On-chip headphone driver 40mW output power
- Microphone interface
- Pop and click suppression

Please refer to the WM8960 datasheet for additional details.

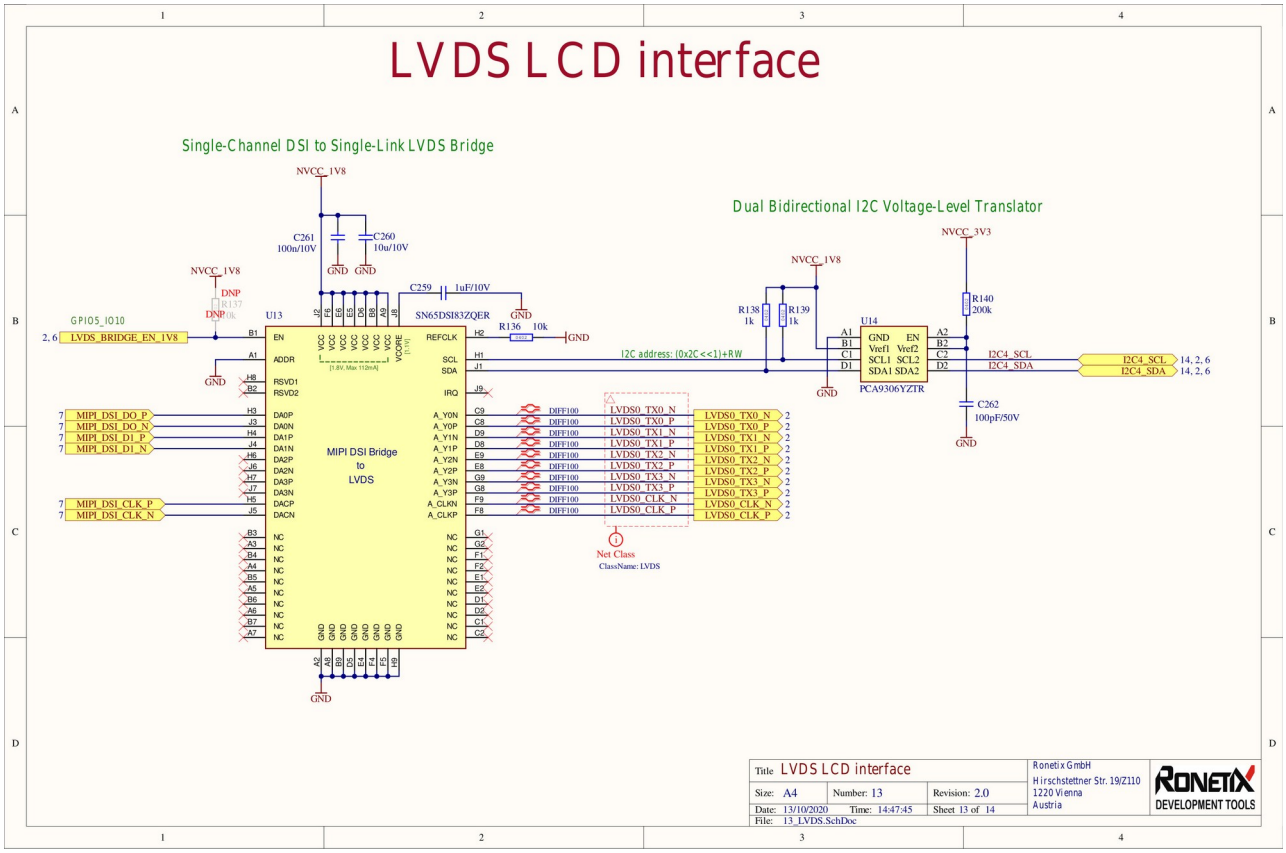
If the WM8960 is not populated, the SAI signals can be bypassed to the SODIMM204 connector. Either the speaker or the headphone signals can be provided to the SODIMM204 connector.



4.7 LVDS bridge

i.MX7-CM implements (optional) onboard LVDS display interface by converting the MIPI-DSI to LVDS signals using Texas Instruments SN65DSI83 transceiver with following main features:

- LVDS Output Clock Range of 25 MHz to 154MHz.
- Suitable for 60 fps 1366 x 768 / 1280 x 800 at 18 bpp and 24 bpp.
- ESD Rating ±2 kV



4.8 LED

The i.MX7-CM features a red LED controlled by GPIO2_IO07 signal of the i.MX7. The LED is ON when GPIO2_IO07 is logic Low.

5. SODIMM204 connector

The i.MX7-CM exposes a 204 pin SO-DIMM connector.

Recommended mating Connector socket for custom board interfacing are the following connectors (or equivalent):

- TE Connectivity 2013289-2 or 2013289-1
- Cvilux CS69-2042CA0-R0
- JAE MM80-204B1-1

Pin	Signal	i.MX7 Ball	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5	Alt-6	Alt-7	Alt-8
1	GND										
3	GPIO1_IO03	N05	gpio1.IO[3]	pwm3.OUT		sai3.MCLK	osc32k.32K_OUT	ccm-CLKO2			
5	GPIO1_IO09	R2	gpio1.IO[9]	usdhc1.LCTL		uart3.TX	i2c3.SDA	gpc.PMIC_RDY		pwm2-OUT	
7	GPIO1_IO12	T2	gpio1.IO[12]	usdhc2.VSELECT		can1.RX		ccm.EXT_CLK1		usb_OTG1_ID	
9	GPIO1_IO13	T3	gpio1.IO[13]	usdhc3.VSELECT		can1.TX	gpc.PMIC_RDY	ccm.EXT_CLK2		usb_OTG2_ID	
11	ETH2_TX1_P										
13	ETH2_TX1_N										
15	ETH2_RX1_P										
17	ETH2_RX1_N										
19	ETH2_TX2_P										
21	ETH2_TX2_N										
23	ETH2_RX2_P										
25	ETH2_RX2_N										
27	ETH2_LED2										
29	ETH2_LED1										
31	GND										
33	USB_OTG2_VBUS	C10									
35	USB_OTG2_N	A10									
37	USB_OTG2_P	B10									
39	USB_OTG2_ID	B11									
41	GND										
43	USB_OTG1_VBUS	C8									
45	USB_OTG1_N	A8									
47	USB_OTG1_P	B8									
49	USB_OTG1_ID	B7									
51	GND										
53	ETH1_TX1_P										
55	ETH1_TX1_N										
57	ETH1_RX1_P										
59	ETH1_RX1_N										
61	ETH1_TX2_P										
63	ETH1_TX2_N										
65	ETH1_RX2_P										
67	ETH1_RX2_N										
69	ETH1_LED2										
71	ETH1_LED1										
73	ESPI3_SS2_1V8	D3	usdhc2.CD_B	enet1.MDIO	enet2.MDIO	ecspi3.SS2		gpio5.IO[9]			
75	LVDS_BRIDGE_EN_1V8	C3	usdhc2.WP	enet1.MDC	enet2.MDC	ecspi3.SS3	usb.OTG1_ID	gpio5.IO[10]			
77	USR_BT0_1V8	G3	usdhc2.RESET_B	sai2.MCLK	usdhc2.RESET	ecspi3.RDY	usb.OTG2_ID	gpio5.IO[11]			
79	GND										
81	ESPI3_SS0	E8	sai2.TX_DATA[0]	ecspi3.SS0	uart4.RTS_B	uart2.RTS_B	flextimer2.CH[7]	gpio6.IO[22]	kpp.ROW[7]		
83	ESPI3_SCLK	E9	sai2.RX_DATA[0]	ecspi3.SCLK	uart4.CTS_B	uart2.CTS_B	flextimer2.CH[6]	gpio6.IO[21]	kpp.COL[7]		
85	ESPI3_MOSI	D8	sai2.TX_BCLK	ecspi3.MOSI	uart4.TX	uart1.RTS_B	flextimer2.CH[5]	gpio6.IO[20]			
87	ESPI3_MISO	D9	ai2.TX_SYNC	ecspi3.MISO	uart4.RX	uart1.CTS_B	flextimer2.CH[4]	gpio6.IO[19]			
89	GND										
91	LVDS0_TX3_P										
93	LVDS0_TX3_N										
95	LVDS0_CLK_P										
97	LVDS0_CLK_N										
99	LVDS0_TX2_P										
101	LVDS0_TX2_N										
103	LVDS0_TX1_P										
105	LVDS0_TX1_N										
107	LVDS0_TX0_P										
109	LVDS0_TX0_N										
111	GND										
113	AUDIO_MCLK_R										
115	SPK_RN										
117	MIC										
119	SPK_RP										
121	HEADPHONE_L										
123	HEADPHONE_R										
125	I2C2_SCL	K2	i2c2.SCL	uart4.RX	wdog3.WDOG_B	ecspi3.SCLK	ccm.ENET2_REF_CLK_ROOT	gpio4.IO[10]	usdhc3.CD_B		
127	I2C2_SDA	K3	i2c2.SDA	uart4.TX	wdog3.WDOG_RST_B_DEB	ecspi3.SS0	ccm.ENET3_REF_CLK_ROOT	gpio4.IO[11]	usdhc3.WP		
129	I2C3_SCL	K5	i2c3.SCL	uart5.CTS_B	can2.RX	csi1.VSYNC	sdma.EXT_EVENT[0]	gpio4.IO[12]	epdc.BDR[0]		
131	I2C3_SDA	K6	i2c3.SDA	uart5.RTS_B	can2.TX	csi1.HSYNC	sdma.EXT_EVENT[1]	gpio4.IO[13]	epdc.BDR[1]		
133	I2C4_SCL	C12	sai1.RX_SYNC	rawnand.CE2_B	sai2.RX_SYNC	i2c4.SCL	sim1.PORT1_PD	gpio6.IO[16]	mqs.RIGHT		
135	I2C4_SDA	D12	sai1.RX_BCLK	rawnand.CE3_B	sai2.RX_BCLK	i2c4.SDA	flextimer2.PHA	gpio6.IO[17]			
137	UART1_RXD	L3	uart1.RX	i2c1.SCL	gpc.PMIC_RDY	ecspi1.SS1	enet2.1588_EVENT0_IN	gpio4.IO[0]	enet1.MDIO		
139	UART1_TXD	L4	uart1.TX	i2c1.SDA	sai3.MCLK	ecspi1.SS2	enet2.1588_EVENT0_OUT	gpio4.IO[1]	enet1.MDC		
141	UART2_RXD	L5	uart2.RX	i2c2.SCL	sai3.RX_BCLK	ecspi1.SS3	enet2.1588_EVENT1_IN	gpio4.IO[2]	enet2.MDIO		
143	UART2_TXD	L6	uart2.TX	i2c2.SDA	sai3.RX_DATA[0]	ecspi1.RDY	enet2.1588_EVENT1_OUT	gpio4.IO[3]	enet2.MDC		
145	GND										
147	ADC1_IN0_1V8	AD1									
149	ADC1_IN1_1V8	AD3									
151	ADC1_IN2_1V8	AE2									
153	ADC1_IN3_1V8	AE3									
155	ADC2_IN0_1V8	AC1									
157	ADC2_IN1_1V8	AC2									
159	ADC2_IN2_1V8	AB1									
161	ADC2_IN3_1V8	AB2									
163	VSNVS										
165	PMIC_PWRON										
167	MX7_ONOFF	AC8									
169	JTAG_TCK	U5									
171	JTAG_TDI	U3									
173	JTAG_TDO	U6									
175	JTAG_TMS	U4									
177	JTAG_TRST_B	U2									
179	POR_B	R6									
181	CAN2_RX	T5	gpio1.IO[14]	usdhc3.CD_B	enet2.MDIO	can2.RX	wdog3.WDOG_B	ccm.EXT_CLK3	sdma.EXT_EVENT[0]		
183	CAN2_TX	T6	gpio1.IO[15]	usdhc3.WP	enet2.MDC	can2.TX	wdog4.WDOG_B	ccm.EXT_CLK4	sdma.EXT_EVENT[1]		
185	LICELL										
187	BOARD_DETECT										
189	NVCC_3V3	Provided to i.MX7-MB									
191	VIN(3V5-4V2)										
193	VIN(3V5-4V2)										
195	VIN(3V5-4V2)										
197	VIN(3V5-4V2)										
199	VIN(3V5-4V2)										
201	GND										
203	GND										

Pin	Signal	i.MX7 Ball	Alt-0	Alt-1	Alt-2	Alt-3	Alt-4	Alt-5	Alt-6	Alt-7	Alt-8
2	GND										
4	GPIO1_IO00	N1	gpio1.IO[0]	pwm4.OUT	global wdog	wdog1.WDOG_B	wdog1.WDOG_RST_B_DEB	gpc.REF_EN_B			
6	GPIO1_IO01	N2	gpio1.IO[1]	pwm1.OUT	ccm.ENET3_REF_CLK_ROOT	sai1.MCLK	anatop.24M_OUT	ccm.OUT0			
8											
10	GPIO2_IO30	H24	epdc.PWRCOM	flextimer2.PHA	enet2.CRS		weim.AD[9]	gpio2.IO[30]	lcdif.HSYNC	lcdif.DATA[11]	
12	GPIO4_IO14	L1	i2c4.SCL	uart5.RX	wdog4.WDOG_B	csi1.PIXCLK	usb.OTG1_ID	gpio4.IO[14]	epdc.VCOM[0]		
14	GPIO4_IO15	L2	i2c4.SDA	uart5.TX	wdog4.WDOG_RST_B_DEB	csi1.MCLK	usb.OTG2_ID	gpio4.IO[15]	epdc.VCOM[1]		
16											
18	GPIO4_IO07	M6	uart3.CTS_B	usb.OTG2_PWR	sai3.TX_SYNC	ecspi1.SS0	enet1.1588_EVENT1_OUT	gpio4.IO[7]	usdhc1.VSELECT		
20	GPIO6_IO12	E12	sai1.RX_DATA[0]	rawnand.CE1_B	uart5.RX	can1.RX	sim1.PORT1_TRXD	gpio6.IO[12]			
22	GPIO6_IO13	C11	sai1.TX_BCLK	rawnand.CE0_B	uart5.TX	can1.TX	sim1.PORT1_CLK	gpio6.IO[13]			
24	GPIO6_IO14	D11	sai1.TX_SYNC	rawnand.DQS	uart5.CTS_B	can2.RX	sim1.PORT1_RST_B	gpio6.IO[14]			
26	GPIO6_IO15	E11	sai1.TX_DATA[0]	rawnand.READY_B	uart5.RTS_B	can2.TX	sim1.PORT1_SVEN	gpio6.IO[15]			
28	GND										
30	MIPI_CSI_CLK_P	B15									
32	MIPI_CSI_CLK_N	A15									
34	MIPI_CSI_DO_P	B16									
36	MIPI_CSI_DO_N	A16									
38	MIPI_CSI_D1_P	B14									
40	MIPI_CSI_D1_N	A14									
42	SD1_DATA0	A5	usdhc1.DATA0	sai3.RX_DATA[0]	uart7.RX	ecspi4.SS2	flextimer2.CH[1]	gpio5.IO[5]	ccm.EXT_CLK1		
44	SD1_CMD	C5	usdhc1.CMD	sai3.RX_BCLK		ecspi4.SS1	flextimer2.CH[0]	gpio5.IO[4]	ccm.OUT2		
46	GND										
48	SD1_CLK	B5	usdhc1.CLK	sai3.RX_SYNC	uart6.CTS_B	ecspi4.SS0	flextimer1.CH[3]	gpio5.IO[3]	ccm.OUT1		
50	SD1_DATA1	D6	usdhc1.DATA1	sai3.TX_BCLK	uart7.TX	ecspi4.SS3	flextimer2.CH[2]	gpio5.IO[6]	ccm.EXT_CLK2		
52	SD1_CD_B	C6	usdhc1.CD_B		uart6.RX	ecspi4.MISO	flextimer1.CH[0]	gpio5.IO[0]	ccm.CLKO1		
54	SD1_DATA2	A4	usdhc1.DATA2	sai3.TX_SYNC	uart7.CTS_B	ecspi4.RDY	flextimer2.CH[3]	gpio5.IO[7]	ccm.EXT_CLK3		
56	SD1_DATA3	D5	usdhc1.DATA3	sai3.TX_DATA[0]	uart7.RTS_B	ecspi3.SS1	flextimer1.PHA	gpio5.IO[8]	ccm.EXT_CLK4		
58	SD1_WP	C4	usdhc1.WP		uart6.TX	ecspi4.MOSI	flextimer1.CH[1]	gpio5.IO[1]	ccm.CLKO2		
60	SD1_RESET_B	B4	usdhc1.RESET_B	sai3.MCLK	uart6.RTS_B	ecspi4.SCLK	flextimer1.CH[2]	gpio5.IO[2]	ccm.OUT0		
62	NVCC_SD1	Provided to i.MX7-MB									
64	GND										
66	USB_OTG2_OC	P2	gpio1.IO[6]	usb.OTG2_OC	flextimer1.CH[6]	uart5.RX	i2c2.SCL	gpc.WAIT	kpp.ROW[4]		
68	USB_OTG2_PWR	P3	gpio1.IO[7]	usb.OTG2_PWR	flextimer1.CH[7]	uart5.TX	i2c2.SDA	gpc.STOP	kpp.COL[4]		
70	USB_OTG1_OC	N6	gpio1.IO[4]	usb.OTG1_OC	flextimer1.CH[4]	uart5.CTS_B	i2c1.SCL	ccm.OUT1	observe_mux.OUT[3]		
72	USB_OTG1_PWR	P1	gpio1.IO[5]	usb.OTG1_PWR	flextimer1.CH[5]	uart5.RTS_B	i2c1.SDA	ccm.OUT2	observe_mux.OUT[4]		
74	GND										
76	LCD_DAT0	D21	lcdif.DATA[0]	gpt1.COMPARE2	coresight.TRACE[0]	csi1.DATA[20]	weim.DATA[0]	gpio3.IO[5]	src.BT_CFG[0]		
78	LCD_DAT1	A22	lcdif.DATA[1]	gpt1.COMPARE3	coresight.TRACE[1]	csi1.DATA[21]	weim.DATA[1]	gpio3.IO[6]	src.BT_CFG[1]		
80	LCD_DAT2	B22	lcdif.DATA[2]	gpt1.CLK	coresight.TRACE[2]	csi1.DATA[22]	weim.DATA[2]	gpio3.IO[7]	src.BT_CFG[2]		
82	LCD_DAT3	A23	lcdif.DATA[3]	gpt1.CAPTURE1	coresight.TRACE[3]	csi1.DATA[23]	weim.DATA[3]	gpio3.IO[8]	src.BT_CFG[3]		
84	LCD_DAT4	C22	lcdif.DATA[4]	gpt1.CAPTURE2	coresight.TRACE[4]	csi1.VSYNC	weim.DATA[4]	gpio3.IO[9]	src.BT_CFG[4]		
86	LCD_DAT5	B23	lcdif.DATA[5]		coresight.TRACE[5]	csi1.HSYNC	weim.DATA[5]	gpio3.IO[10]	src.BT_CFG[5]		
88	LCD_DAT6	A24	lcdif.DATA[6]		coresight.TRACE[6]	csi1.PIXCLK	weim.DATA[6]	gpio3.IO[11]	src.BT_CFG[6]		
90	LCD_DAT7	F20	lcdif.DATA[7]		coresight.TRACE[7]	csi1.MCLK	weim.DATA[7]	gpio3.IO[12]	src.BT_CFG[7]		
92	GND										
94	LCD_DAT8	E21	lcdif.DATA[8]		coresight.TRACE[8]	csi1.DATA[9]	weim.DATA[8]	gpio3.IO[13]	src.BT_CFG[8]		
96	LCD_DAT9	C23	lcdif.DATA[9]		coresight.TRACE[9]	csi1.DATA[8]	weim.DATA[9]	gpio3.IO[14]	src.BT_CFG[9]		
98	LCD_DAT10	B24	lcdif.DATA[10]		coresight.TRACE[10]	csi1.DATA[7]	weim.DATA[10]	gpio3.IO[15]	src.BT_CFG[10]		
100	LCD_DAT11	G20	lcdif.DATA[11]		coresight.TRACE[11]	csi1.DATA[6]	weim.DATA[11]	gpio3.IO[16]	src.BT_CFG[11]		
102	LCD_DAT12	F21	lcdif.DATA[12]		coresight.TRACE[12]	csi1.DATA[5]	weim.DATA[12]	gpio3.IO[17]	src.BT_CFG[12]		
104	LCD_DAT13	E22	lcdif.DATA[13]		coresight.TRACE[13]	csi1.DATA[4]	weim.DATA[13]	gpio3.IO[18]	src.BT_CFG[13]		
106	LCD_DAT14	D23	lcdif.DATA[14]		coresight.TRACE[14]	csi1.DATA[3]	weim.DATA[14]	gpio3.IO[19]	src.BT_CFG[14]		
108	LCD_DAT15	C24	lcdif.DATA[15]		coresight.TRACE[15]	csi1.DATA[2]	weim.DATA[15]	gpio3.IO[20]	src.BT_CFG[15]		
110	GND										
112	LCD_DAT16	B25	lcdif.DATA[16]	flextimer1.CH[4]	coresight.TRACE_CLK	csi1.DATA[1]	weim.CRE	gpio3.IO[21]	src.BT_CFG[16]		
114	LCD_DAT17	G21	lcdif.DATA[17]	flextimer1.CH[5]	coresight.TRACE_CTL	csi1.DATA[0]	weim.ACLK_FREERUN	gpio3.IO[22]	src.BT_CFG[17]		
116	LCD_DAT18	E23	lcdif.DATA[18]	flextimer1.CH[6]	coresight.EVENTO	csi1.DATA[15]	weim.CS2_B	gpio3.IO[23]	src.BT_CFG[18]		
118	LCD_DAT19	D24	lcdif.DATA[19]	flextimer1.CH[7]		csi1.DATA[14]	weim.CS3_B	gpio3.IO[24]	src.BT_CFG[19]		
120	LCD_DAT20	C25	lcdif.DATA[20]	flextimer2.CH[4]	enet1.1588_EVENT2_OUT	csi1.DATA[13]	weim.ADDR[23]	gpio3.IO[25]	I2C3_SCL		
122	LCD_DAT21	E24	lcdif.DATA[21]	flextimer2.CH[5]	enet1.1588_EVENT3_OUT	csi1.DATA[12]	weim.ADDR[24]	gpio3.IO[26]	I2C3_SDA		
124	LCD_DAT22	D25	lcdif.DATA[22]	flextimer2.CH[6]	enet2.1588_EVENT2_OUT	csi1.DATA[11]	weim.ADDR[25]	gpio3.IO[27]	I2C4_SCL		
126	LCD_DAT23	G23	lcdif.DATA[23]	flextimer2.CH[7]	enet2.1588_EVENT3_OUT	csi1.DATA[10]	weim.ADDR[26]	gpio3.IO[28]	I2C4_SDA		
128	LCD_CLK	E20	ecspi4.MISO	enet1.1588_EVENT2_IN	csi1.DATA[16]	uart2.RX	gpio3.IO[0]				
130	LCD_VSYNC	F24	ecspi4.SS0	enet2.1588_EVENT3_IN	csi1.DATA[19]	uart2.CTS_B	gpio3.IO[3]				
132	LCD_HSYNC	E25	ecspi4.SCLK	enet2.1588_EVENT2_IN	csi1.DATA[18]	uart2.RTS_B	gpio3.IO[2]				
134	LCD_ENABLE	F25	ecspi4.MOSI	enet1.1588_EVENT3_IN	csi1.DATA[17]	uart2.TX	gpio3.IO[1]				
136	LCD_RESET	C21	gpt1.COMPARE1	coresight.EVENTI	csi1.FIELD	weim.DTACK_B	gpio3.IO[4]				
138	GND										
140	PCIE_REFCLK_P	AD10									
142	PCIE_REFCLK_N	AE10									
144	PCIE_REFCLKOUT_P	AB10									
146	PCIE_REFCLKOUT_N	AC10									
148	PCIE_RX_P	AD11									
150	PCIE_RX_N	AE11									
152	PCIE_TX_P	AB11									
154	PCIE_TX_N	AC11									
156	GPIO2_IO08	M23	EPDC_D8	epdc.SDDO[8]	sim1.PORT1_TRXD	qspi.B_DATA[0]	uart6.RX	weim.OE	gpio2.IO[8]	lcdif.DATA[8]	lcdif.BUSY
158	GPIO2_IO09	L25	EPDC_D9	epdc.SDDO[9]	sim1.PORT1_CLK	qspi.B_DATA[1]	uart6.TX	weim.RW	gpio2.IO[9]	lcdif.DATA[9]	lcdif.DATA[0]
160	GPIO2_IO10	L24	EPDC_D10	epdc.SDDO[10]	sim1.PORT1_RST_B	qspi.B_DATA[2]	uart6.RTS_B	weim.CS0_B	gpio2.IO[10]	lcdif.DATA[10]	lcdif.DATA[9]
162	GPIO2_IO11	L23	EPDC_D11	epdc.SDDO[11]	sim1.PORT1_SVEN	qspi.B_DATA[3]	uart6.CTS_B	weim.BCLK	gpio2.IO[11]	lcdif.DATA[11]	lcdif.DATA[1]
164	GPIO2_IO12	L22	EPDC_D12	epdc.SDDO[12]	sim1.PORT1_PD	qspi.B_DQS	uart7.RX	weim.LBA_B	gpio2.IO[12]	lcdif.DATA[12]	lcdif.DATA[21]
166	GPIO2_IO13	L21	EPDC_D13	epdc.SDDO[13]	sim2.PORT1_TRXD	qspi.B_SCLK	uart7.TX	weim.WAIT	gpio2.IO[13]	lcdif.DATA[13]	lcdif.CS
168	GPIO2_IO14	L20	EPDC_D14	epdc.SDDO[14]	sim2.PORT1_CLK	qspi.B_SS0_B	uart7.RTS_B	weim.EB_B[0]	gpio2.IO[14]	lcdif.DATA[14]	lcdif.DATA[22]
170	GPIO2_IO15	K25	EPDC_D15	epdc.SDDO[15]	sim2.PORT1_RST_B	qspi.B_SS1_B	uart7.CTS_B	weim.CS1_B	gpio2.IO[15]	lcdif.DATA[15]	lcdif.WR_RWN
172	GPIO1_IO02	N3	gpio1.IO[2]	pwm2.OUT	ccm.ENET1_REF_CLK_ROOT	sai2.MCLK	anatop.32K_OUT	ccm.CLKO1	observe_mux.OUT[1]	usb.OTG1_ID	
174	GPIO2_IO31	K20	epdc.PWRSTAT	flextimer2.PHB	enet2.COL		weim.EB_B[1]	gpio2.IO[31]	lcdif.VSYNC	lcdif.DATA[12]	
176	GPIO2_IO28	K24	epdc.BDR[0]		enet2.TX_CLK	ccm.ENET2_REF_CLK_ROOT	weim.ADDR[22]	gpio2.IO[28]	lcdif.CS	lcdif.DATA[7]	
178	GPIO2_IO29	K23	epdc.BDR[1]	epdc.SDCLKN	enet2.RX_CLK		weim.AD[8]	gpio2.IO[29]	lcdif.ENABLE	lcdif.DATA[6]	
180	GND										
182	VDD_SNVS_1P8_CAP	AE8									
184	SNVS_TAMPER0	AA7									
186	SNVS_TAMPER1	Y8									
188	SNVS_TAMPER2	AB6									
190	SNVS_TAMPER3	Y7									
192	BOOT_MODE0	P4									
194	BOOT_MODE1	P5									
196	VIN(3V5-4V2)										
198	VIN(3V5-4V2)										
200	VIN(3V5-4V2)										
202	GND										
204	GND										

6. CPU Module interfaces

6.1 Display interfaces

i.MX7-CM provides the following display interfaces:

- LVDS Interface – using Texas Instruments SN65DSI83 MIPI-DSI to LVDS bridge
  - LVDS Output Clock Range of 25 MHz to 154MHz.
  - Suitable for 60 fps 1366 x 768 / 1280 x 800 at 18 bpp and 24 bpp.
  - ESD Rating ±2 kV
- Parallel Display Interface

  i.MX7-CM Parallel display interface is derived from the i.MX7 integrated Enhanced LCD interface (eLCDIF) designed to drive a wide range of display devices varying in size and capabilities. eLCDIF supports the following main features:
  - Support for parallel LCD displays (up to 24-bit) with resolutions up to 1920x1080 at 60Hz.
  - Support for both synchronous and asynchronous “smart” displays.
  - Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
  - ITU-R BT.656 mode, including progressive-to-interlace feature and RGB to YCbCr 4:2:2
  - color space conversion to support 525/60 and 625/50 operation.

  Please refer to the i.MX7 Reference manual for additional details.

6.2 MIPI-CSI Camera interface

The MIPI-CSI interface available with i.MX7-CM is derived from the two-lane MIPI CSI2 host controller (MIPI_CSI2) integrated into the i.MX7 SoC. The CSI2 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between I.MX7-CM and a MIPI CSI-2 compliant camera sensor. The following main features are supported:

- Up-to two data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.

- Compliant to MIPI CSI2 Standard Specification V1.01r06.
- Supports primary and secondary image format:
  - RGB565, RGB666, RGB888
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits.
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14

Please refer to the i.MX7 Reference manual for additional details.

6.3 USB2.0 interface

The i.MX7 SoC is equipped with two high-speed OTG controller modules and integrated high-speed analog USB PHYs. IiMX7-CM enables full access to both ports trough the base board interface connector. The USB ports support the following main features:

- High speed, full speed and low speed operation in host mode.
- High speed and full speed operation in peripheral mode.
- Up to 8 bidirectional endpoints.
- i.MX7-CM USB port 0 (i.MX7 port 1) supports for OTG signaling, session request protocol (SRP), host negotiation protocol (HNP), and attach detection protocol (ADP).
- i.MX7-CM USB port 1 (i.MX7 port 2) is configured to operate in host only mode
- Supports charger detection with USB_OTG1_CHD_B pin (i.MX7 port 1 only) and register interface (both i.MX7 ports)

Please refer to the i.MX7 Reference manual for additional details.

6.4 PCI-Express

The i.MX7 SoC is equipped with a single lane PCI Express port (PCIe) v2.1 port. i.MX7-CM enables access to the CPU PCI-Express port through the base board interface. The PCI Express port supports the following main features:

- Single lane compliant with PCI Express base specification v2.1 (6.0Gbps).
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface.

- Supports spread spectrum clocking in transmitter and receiver.

Please refer to the i.MX7 Reference manual for additional details.

6.5 MMC, SD, SDIO

One MMC/SD/SDIO port is available through the SODIMM204 connector. The port is derived from the i.MX7 on-chip MMC/SD/SDIO controller IPs (uSDHC). The uSDHC supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- Dedicated “card detection” and “write protection” signals
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

Please refer to the i.MX7 Reference manual for additional details.

6.6 UART

The i.MX7-CM exposes up to 6 UART interfaces some of which are muxed with other peripherals.

The i.MX7 UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.

- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

Please refer to the i.MX7 Reference manual for additional details.

6.7 I2C

i.MX7-CM is equipped with three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the i.MX7 Reference manual for additional details.

I2C usage table:

NAME	PERIPHERAL	ADDRESS
I2C1	i.MX7-CM: PMIC control	(0x08<<1)+RW
	i.MX7-CM: EEPROM	(0x50<<1)+RW
	Not available on SODIMM204	
I2C2	i.MX7-MB: PCIe	
	i.MX7-MB: general use on header	
I2C3	i.MX7-MB: MIKROBUS	
	i.MX7-MB: general use on header	
I2C4	i.MX7-CM: Audio Codec	(0x34<<1)+RW
	i.MX7-CM: LVDS	(0x2C<<1)+RW
	i.MX7-MB: PCIe Clock Generator	(0x68<<1)+RW
	i.MX7-MB: CSI (Camera)	(0x3C<<1)+RW
	i.MX7-MB: general use on header	

6.8 SPI

Up-to two SPI interfaces are accessible through the i.MX7-CM base board interface. The SPI interfaces are derived from i.MX7 integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX7 Reference manual for additional details.

6.9 Quad SPI

i.MX7-CM provides one Quad SPI interface (QSPI-B) to the SODIMM204 connector.

QSPI-A is connected onboard to a QSPI NOR Flash.

The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX7 Reference manual for additional details.

6.10 CAN Bus

i.MX7-CM can provide up to 2 CAN interfaces to the SODIMM204 connector.

Each interface is implemented with the i.MX7 integrated FlexCAN module. The following features are supported by the DCAN module:

- Supports CAN protocol version 2.0B.
- Programmable bit rate up to 1 Mbps.
- Flexible Mailboxes of eight bytes data length
- 100% backwards compatibility with previous FLEXCAN version

Please refer to the i.MX7 Reference manual for additional details.

6.11 ADC

i.MX7-CM is equipped with two instances of the general purpose ADC controller. Each instance is implemented with the i.MX7 integrated 12-bit general purpose analog to digital converter module (ADC). The i.MX7 ADC module supports the following main features:

- 12-bit word size.
- Support single and continuous conversion.
- Support compare mode and channel auto disable if data match the requirement.
- Support average conversion and flexible 4, 8, 16, 32 number of conversion data.
- Configurable sample time and conversion speed / power. Sample rates up to 1MHz.
- Conversion complete, hardware average complete, compare, DMA, time out flag and interrupt.
- Automatic compare with interrupt for less than, greater than, and equal to, within range, or out-of-range, programmable value

Please refer to the i.MX7 Reference manual for additional details.

6.12 PWM

Up to four PWM output signals are available at the i.MX7-CM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead

- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX7 Reference manual for additional details.

6.13 FlexTimer

External signals for two integrated flexible time module (FTM) are accessible on the SODIMM204 connector. The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The following features are supported:

- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128.
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode.
- In output compare mode the output signal can be set, cleared, or toggled on match.
- All channels can be configured for center-aligned PWM mode.
- Quadrature decoder with input filters, relative position counting, and interrupts on position count or capture of position count on external event.
- Backwards compatible with TPM.
- Software control of PWM outputs.

Please refer to the i.MX7 Reference manual for additional details.

6.14 Watchdog Timers

Up to four “Watchdog timers” (WDOG) are available on the SODIMM204 connector. The WDOG can be used to protect system from failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a timeout, the WDOG will assert the internal system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. WDOG supports the following main features:

- A configurable timeout counter with periods from 0.5 seconds up to 128 seconds.
- Time resolution of 0.5 seconds

- Programmable interrupt generation prior to timeout

Please refer to the i.MX7 Reference manual for additional details.

6.15 GPIO

Up-to 96 of the i.MX7 general purpose input/output (GPIO) signals are available on the SODIMM204 connector. When configured as an output, it is possible to write to an i.MX7 register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX7 register. In addition GPIOs peripheral can produce interrupts.

6.16 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the SODIMM204 connector.

7. Power Supply

7.1 Power supply from base board

i.MX7-CM is powered by regulated DC supply 3.5-4.5V

Signal	Type	Description
VIN(3V5-4V2)	Power input	Main Power Supply 3.5-4.5V
LICELL	Power input	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave floating if unused.
GND	Power input	Common ground

7.2 Power supply provided to base board

i.MX7-CM provides some power supplies to the SODIMM204 connector.

Signal	Type	Description
NVCC_3V3	Power output	3.3V, Max. 100mA

Signal	Type	Description
VSNVS	Power output	3.0V, Max 1mA
NVCC_SD1	Power output	3.3V or 1.8V, Max. 100mA
VDD_SNVS_1P8_CAP	Power output	1.8V used by the tamper inputs

7.3 System Signals

Signal	Type	Description
MX7_ONOFF	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
PMIC_PWRON	Input	PMIC Power On signal
POR_B	Input, Output	I.MX7 CPU Power On Reset input signal, PMIC Reset open drain output signal. ‘0’ logic will reset the system
BOARD_DETECT		1.5k, 1% resistor connected to GND. Can be used for CPU Module detecting or version coding.

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	Mln	Max	Unit
VIN(3V5-4V2) – Main Power Supply	-0.3	4.8	V
LICELL - Backup battery supply	-0.3	3.6	V
USB_VBUS - USB_HOST_VBUS, USB_OTG_VBUS	-0.3	5.25	V

8.2 Recommended Operating Conditions

Parameter	MIn	Typ	Max	Unit
VIN(3V5-4V2) – Main Power Supply	3.5		4.5	V
VIN(3V5-4V2) – recommended source capability		1.5		A
LICELL - Backup battery supply	1.8	3.0	3.3	V

9. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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