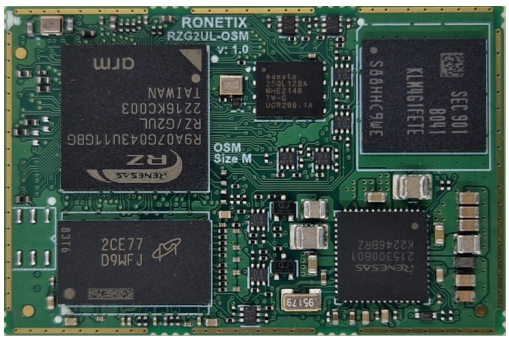
High-performance System on Module (SOM)

RNX-RZG2UL-OSM

Open Standard Module with Renesas RZ/G2UL

Datasheet

rev 1.0



Ronetix Development Tools GmbH
Hirschstettner Str. 19/Z110
1220 Vienna
Austria
www.ronetix.at

1. Document Revision History

Revision	Date	Notes
1.0	07-Nov-2023	Initial release

2. Table of Contents

Table of Contents

1. Document Revision History....3
2. Table of Contents....3
3. Overview....5
3.1 General Information....5
3.2 Highlights....6
3.3 SoM Block Diagram....7
4. CPU Module Hardware Components....8
4.1 Power supply....8
4.2 CPU RZ/G2UL....8
4.2.1 CPU Block Diagram....9
4.2.2 CPU Platform....9
4.3 Memory....10
4.3.1 DRAM....10
4.3.2 eMMC – non-volatile storage memory....10
4.4 USB Hub....10
4.5 GPIO Expander....10
5. Open Standard Module LGA 662 contacts....10
6. CPU Module interfaces....11
6.1 Gigabit Ethernet....11
6.2 Display interfaces....11
6.3 MIPI-CSI Camera interface....12
6.4 USB interface....13
6.5 MMC, SD, SDIO....14
6.6 UART....15
6.7 I2C....16
6.8 SPI....17

6.9 PWM....17
6.10 GPIO....18
6.11 JTAG....18
7. Power Supply....19
7.1 Power supply from base board....19
7.2 System Signals....19
8. Electrical Specifications....19
8.1 Absolute maximum ratings....19
8.2 Recommended Operating Conditions....20
9. Operating Temperature Ranges....20
10. Warranty Terms....20

3. Overview

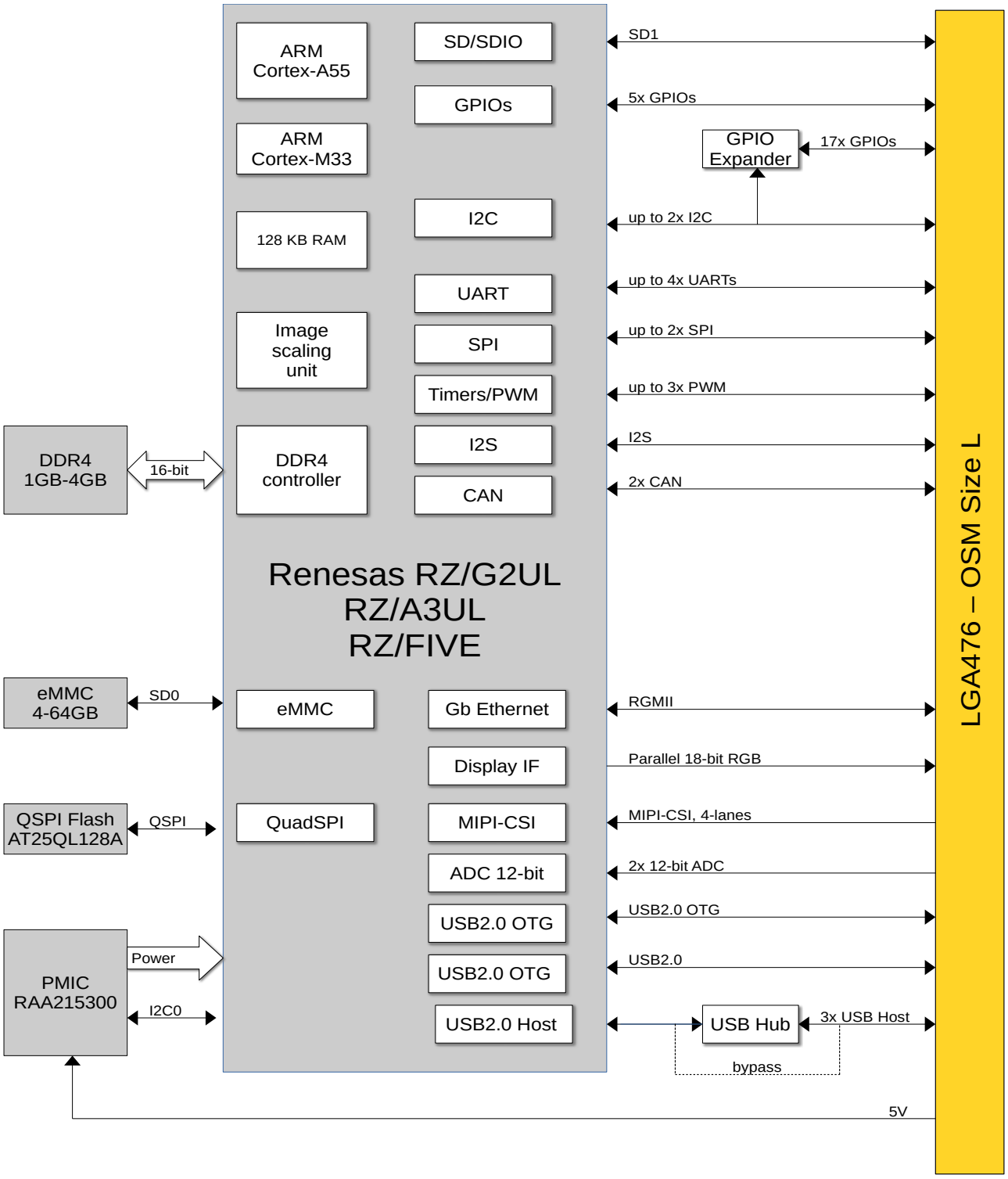
3.1 General Information

The **RNX-RZG2UL-OSM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the Renesas RZ/G2UL family of multipurpose processors from which feature an ARM® Cortex™-A55 up to 1GHz + an additional ARM Cortex-M33 at 200 MHz. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A55 core and an RTOS like FreeRTOS™ on the Cortex-M33 core for time and security critical tasks.

3.2 Highlights

CPU	• Armv8.2-A, 64-bit Cortex™-A55 Core, 1GHz • ARM® Cortex™-M33, 200MHz
Memory	• RAM: 1 GiB LPDDR4 (optional: up to 4 GiB) • eMMC: 4 GiB (optional: up to 64 GiB)
Display	• LCD, parallel 18-bit, RGB
Camera	• MIPI-CSI, 4 data lanes
Network	• Ethernet: 1x RGMII
I/O	• 1x USB2.0 OTG port • 1x or 3x USB2.0 Host port • Up to 4x UART ports • MMC/SD/SDIO • Up to 2x SPI • Up to 2x I2C • Up to 3x general purpose PWM signals • 20x GPIOs
Electrical	• Supply Voltage: 5.0V
Physical	• Board size: Open Standard Module, Size-L, 45x45mm • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of RNX-RZG2UL-OSM SoM.

4.1 Power supply

RNX-RZG2UL-OSM SoM uses Renesas's RAA215300 as a Power Management Integrated circuit (PMIC) designed specifically for use with Renesas's RZ series of application processors. The PMIC regulates all power rails required on CPU module from a single 5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU RZ/G2UL

The RZ/G2UL includes powerful an Arm® Cortex®-A55 processors with speeds up to 1 GHz. A general-purpose Arm® Cortex®-M33 running up to 200 MHz is for real-time and low-power processing. Robust control networks are possible via CAN-FD interface. The RZ/G2UL industrial qualified part is particularly useful for applications such as:

- entry-class industrial gateway control
- Industrial human machine interface (HMI)
- Scanning and printing
- EV Charging
- Industrial automation
- Touchless access control
- Energy meter
- Energy grid equipment

4.2.1 CPU Block Diagram

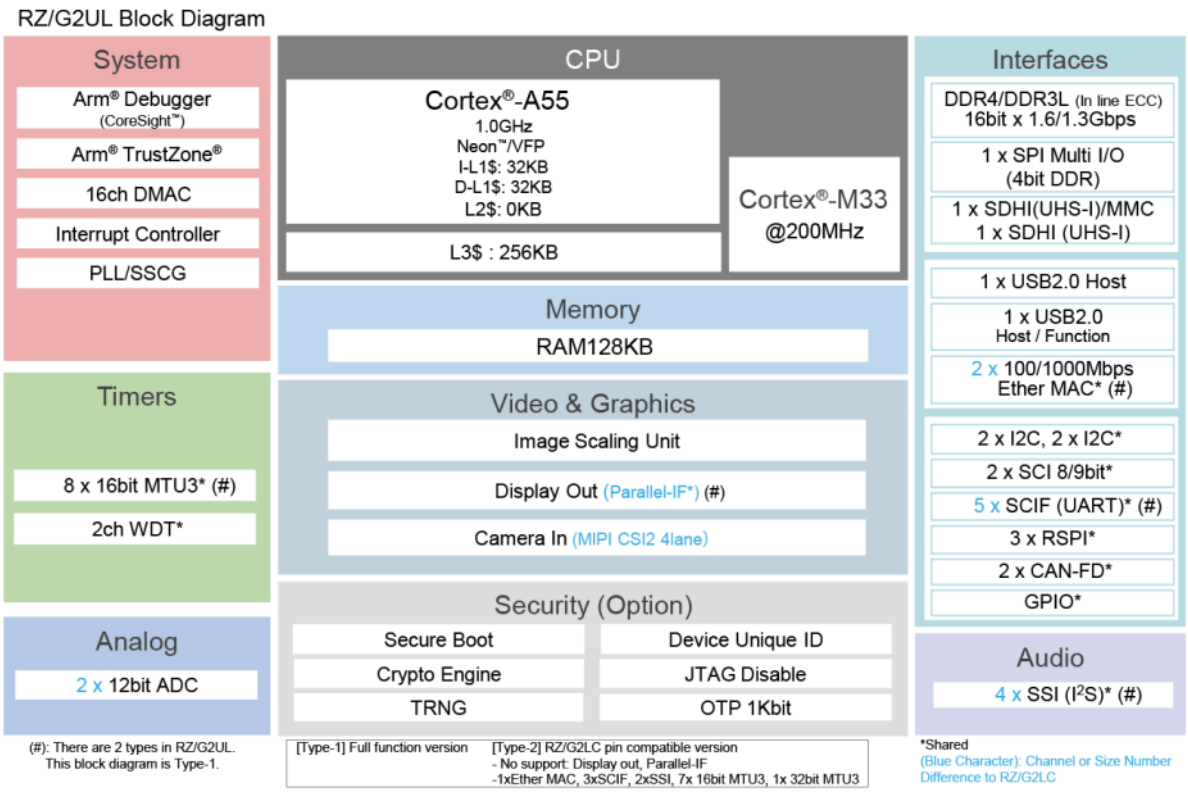


Figure 4.1: RZ/G2UL block diagram

4.2.2 CPU Platform

The RZ/G2UL processor implements an ARM® Cortex®-A55 core intended for high level O/S, with an ARM® Cortex®-M33 core dedicated for real-time and security tasks.

The ARM Cortex-A55 platform has the following features:

- one ARM Cortex-A55 core
- Target frequency of 1GHz
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture

- 128kB L3 cache
- Error Correcting Code (ECC) for On-Chip RAM

The ARM Cortex-M33 platform includes the following features:

- Microcontroller available both for boot and for customer application
- Cortex-M33 CPU core operating at 200 MHz
- Armv8-M security extension
- Secure protected memory regions - 16

4.3 Memory

4.3.1 DRAM

RNX-RZG2UL-OSM SoM is standard equipped with 1 GB DDR4 memory. Optionally up to 2 GB can be assembled. The data bus is 16-bit wide.

4.3.2 eMMC – non-volatile storage memory

RNX-RZG2UL-OSM SoM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.4 USB Hub

An optional USB Hub USB2534, connected to USB1, can be populated. In this case 3 additional USB ports are available on the LGA contacts.

4.5 GPIO Expander

An optional GPIO expander PCAL6416 can be populated. PCAL6416 is connected to I2C0 interface.

5. Open Standard Module LGA 662 contacts

The RNX-RZG2UL-OSM SoM exposes on bottom side 662 LGA constants.

6. CPU Module interfaces

6.1 Gigabit Ethernet

On RNX-RZG2UL-OSM SoM one RGMII 10/100/1000Mbps interface is available on LGA662 contacts. The interface supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Transmission/Reception Low Power Idle Code
- Internal TCP/IP Offload Engine (TOE)
  - Calculation of Checksum of frames for IPv4 and IPv6
  - Filtering of Ethernet Frames

6.2 Display interfaces

RNX-RZG2UL-OSM SoM provides a LCD parallel RGB display interface:

- Parallel, 18-bit, the signals are available on the OSM LGA contacts.
- Supporting WXGA (1280 pixels × 800 lines) for Parallel Output

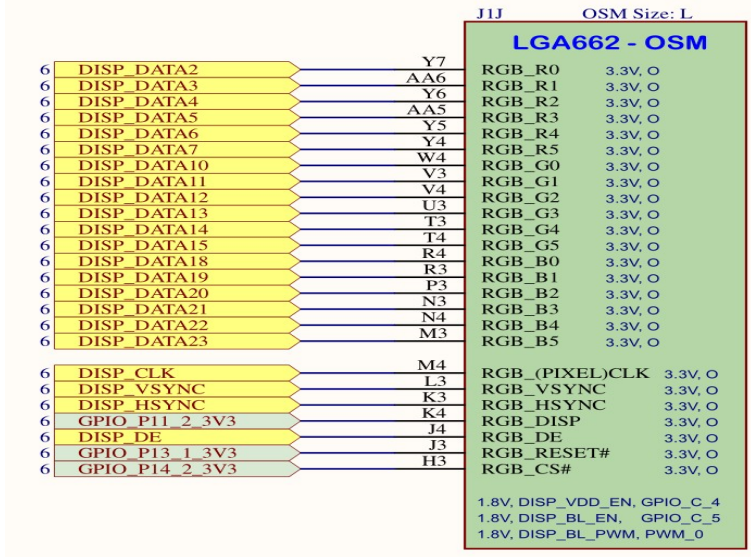


Figure 6.1: LCD Interface – OSM pads

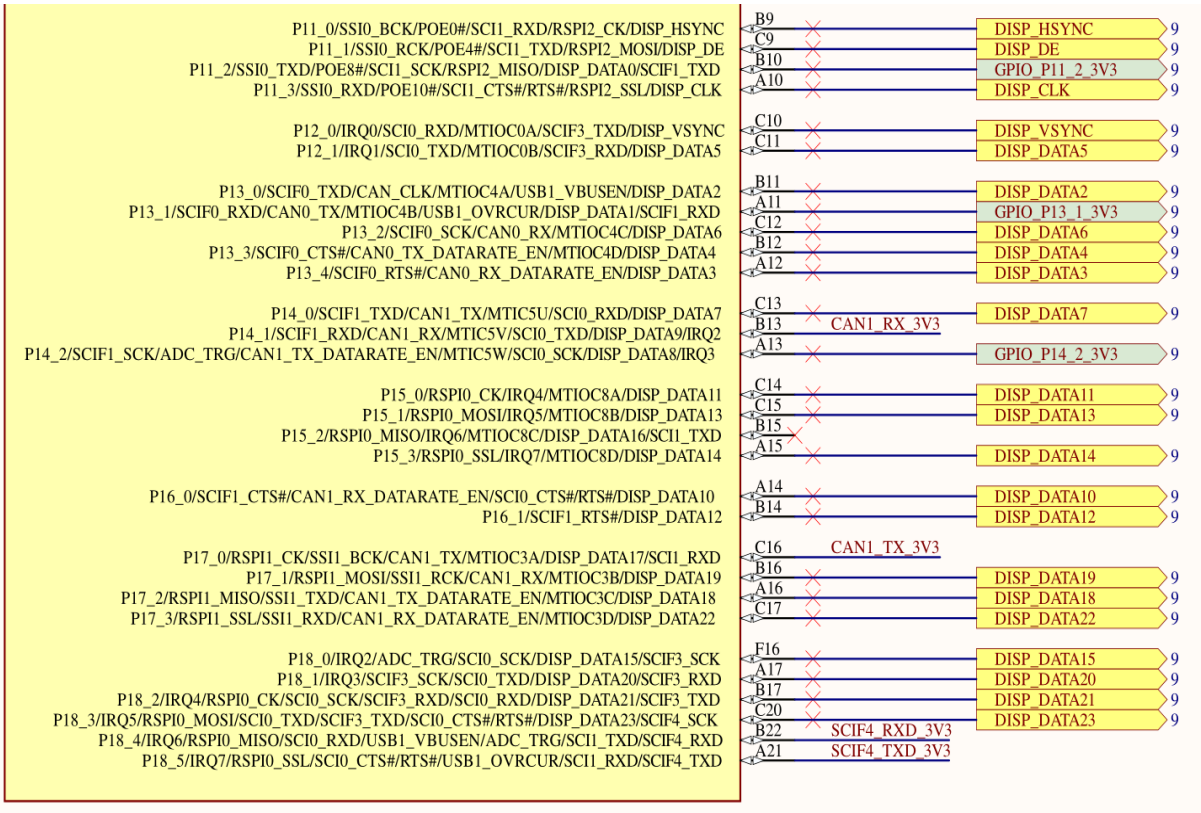


Figure 6.2: LCD Interface – CPU signals

6.3 MIPI-CSI Camera interface

The MIPI-CSI interface is based on the four-lane MIPI camera interface available with the RZ/G2UL SoC. The CSI signals are available on the OSM LGA contacts.

The MIPI Rx D-PHY includes the following features:

- MIPI CSI-2 is an MIPI Camera Serial Interface 2 receiver module
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Maximum image size: 5 M pixels
- Minimum image size: QVGA (320 × 240) = 76.8 K pixels
- Support 1/2/4 lanes
- Support Data De-Scrambling
- Support Latency Reduction and Transport Efficiency (LRTE)

- Support 4 Virtual Channel
- Support Data Interleaving
- Skew Adjustment for D-PHY

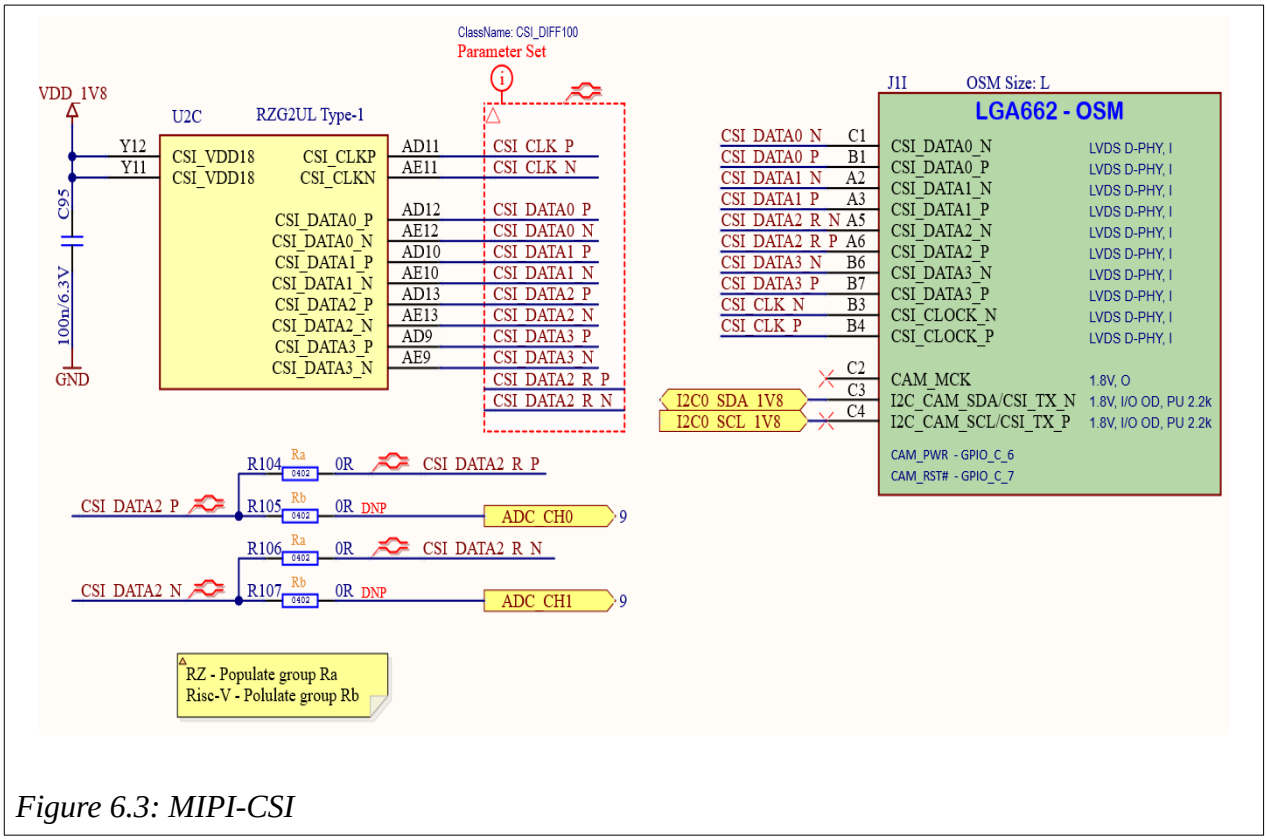


Figure 6.3: MIPI-CSI

6.4 USB interface

The RZ/G2UL SoC is equipped with one USB OTG and one USB Host controllers and PHYs. Each USB instance contains a USB 2.0 core. The USB OTG port supports dual-role functionality.

On RNX-RZG2UL-OSM USB1 is available on the OSM LGA contacts. USB2 can be connected to the OSM LGA contacts or connected to a 4-port USB Hub. In the second case, USBHUB1, USBHUB2 and USBHUB3 are connected to the OSM LGA contacts, the USBHUB4 is not used.

The USB ports support the following main features:

- High-Speed/Full-Speed/Low-Speed OTG core
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol

- up to 8 endpoints
- Low-power mode with local and remote wake-up capability

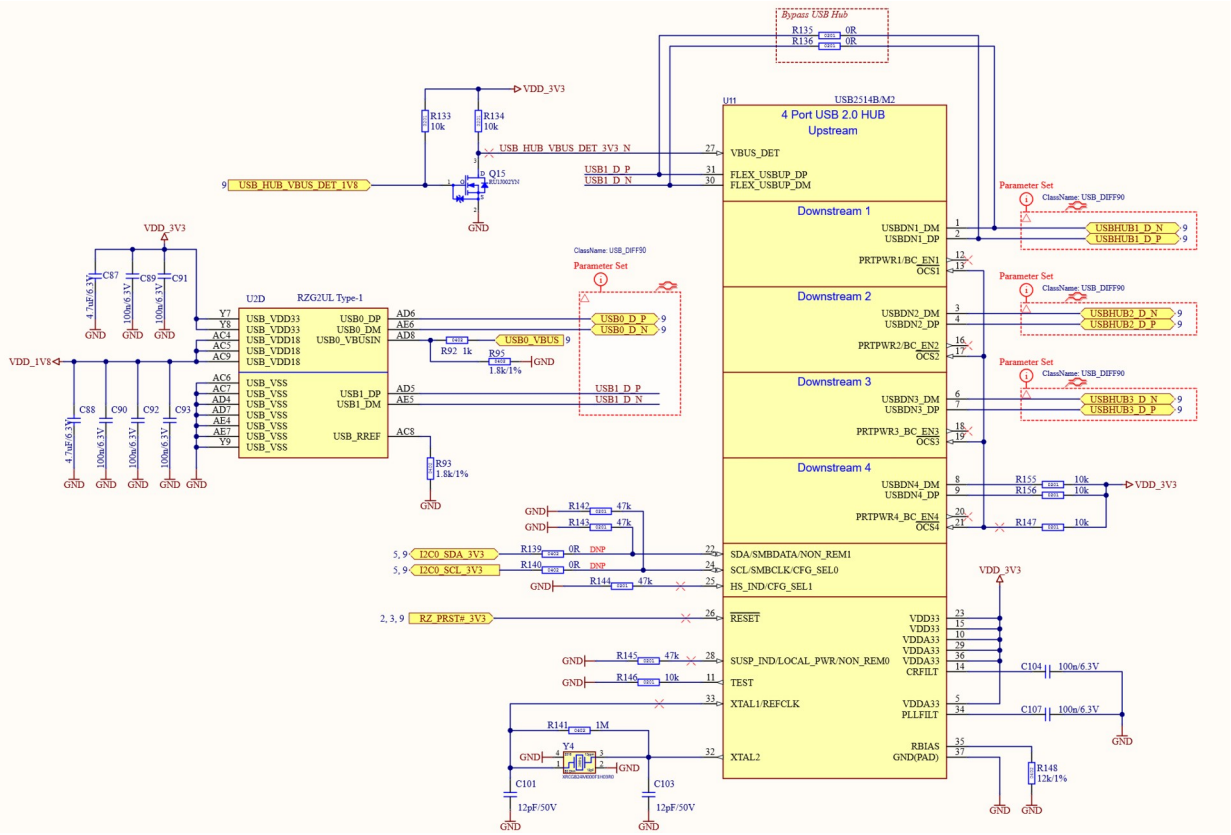


Figure 6.4: USB

6.5 MMC, SD, SDIO

The RZ/G2UL SoC is equipped with two MMC/SD/SDIO controller IPs. On RNX-RZG2UL-OSM SoM SD0 is connected to the eMMC, SD1 is available on the LGA contacts.

The uSDHC supports the following main features:

- Compliant with SD 3.0
- Compliant with eMMC 4.51
- High-speed, HS200 transfer modes supported

- Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported
- SD memory I/O card interface (1-bit / 4-bit SD bus)
- Error check function: CRC7 (Command), CRC16 (Data)
- Card detection function, write protect supported
- MMC interface (1-bit / 4-bit / 8-bit MMC bus)

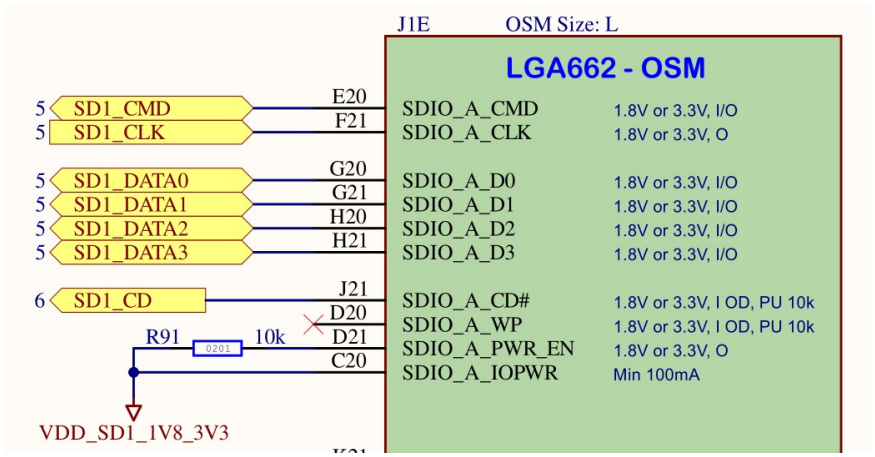


Figure 6.5: SD1 on OSM pads

6.6 UART

The RNX-RZG2UL-OSM SoM exposes 4 UART interfaces.

The RZ/G2UL supports the following features:

- Clock synchronous mode or asynchronous mode selectable
- Simultaneous transmission and reception (full-duplex communication) supported
- Dedicated baud rate generator
- Separate 16-byte FIFO registers for transmission and reception
- Modem control function (channel 0, 1, and 2 in asynchronous mode)

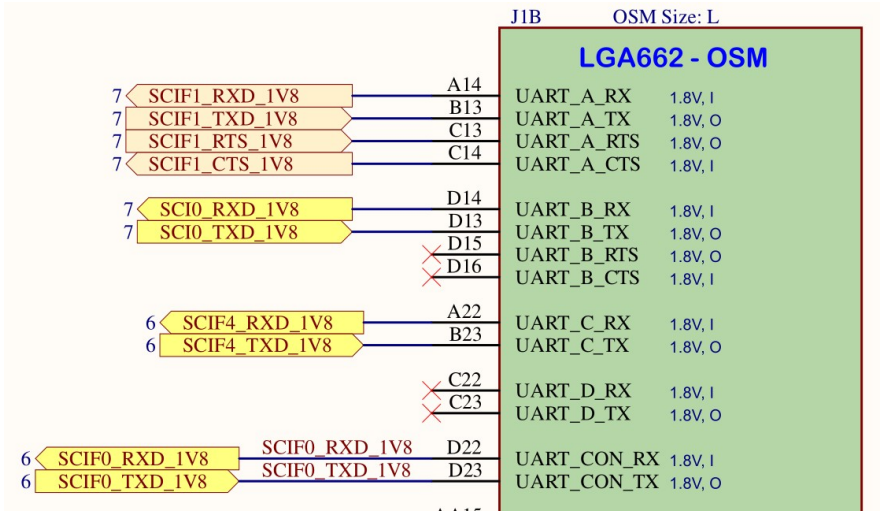


Figure 6.6: UARTs

6.7 I2C

The RZ/G2UL SoC is equipped with four I2C bus interfaces. I2C0 and I2C1 are available on the LGA contacts. I2C0 is used internally to the PMIC, GPIO Expander and USB Hub. The following general features are supported by all I2C bus interfaces:

- Master mode and slave mode supported
- Support for 7-bit and 10-bit slave address formats
- Support for multi-master operation
- Timeout detection

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C0 1.8V	*PMIC*	*(0x12<<1)+RW*
	GPIO Expander	*(0x20<<1)+RW*
	OSM - CSI	
	OSM - I2C_A	
I2C1 1.8V	*OSM - I2C_B*	

Figure 6.7: I2C address usage

6.8 SPI

Two SPI interfaces are accessible through the RNX-RZG2UL-OSM SoM base board interface. The SPI interfaces are derived from RZ/G2UL integrated synchronous serial interface). Each instance of SPI port can operate as either a master or as an SPI slave. The following features are supported:

- Master mode and slave mode supported
- Programmable bit length, clock polarity, clock phase can be selected
- Consecutive transfers
- LSB first / MSB first selectable
- Maximum transfer rate: 33 Mbps

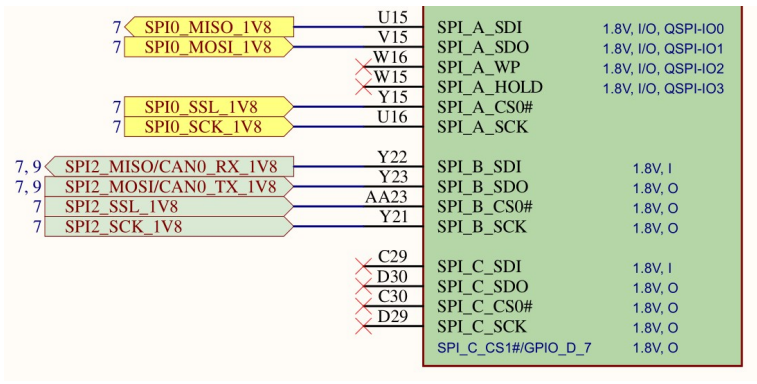


Figure 6.8: SPI on OSM pads

6.9 PWM

Up to three PWM output signals are available at the RNX-RZG2UL-OSM SoM base board interface. The following key features are supported:

- Module clock frequency (P0ϕ): 100 MHz
- 14 types of count clocks selectable
- 39 outputs compare and input capture registers
- Counter clear operation
- Simultaneous writing to multiple timer counters
- 43 types of interrupt sources

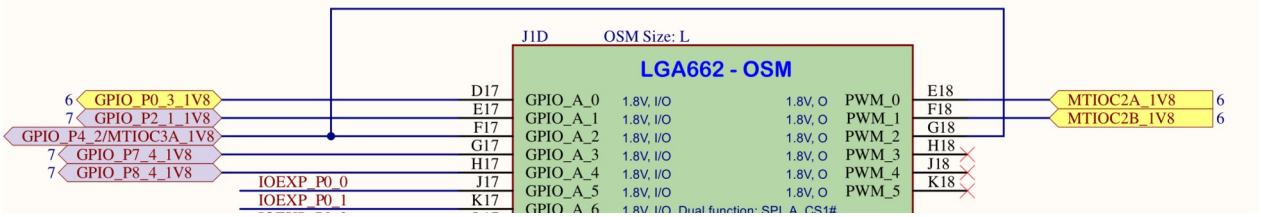


Figure 6.9: PWM on PSM pads

6.10 GPIO

5 of the RZ/G2UL general purpose input/output (GPIO) signals are available on the LGA contacts. Another 17 GPIO of the GPIO I2C expander are available on the OSM pads. When configured as an output, it is possible to write to an RZ/G2UL register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an RZ/G2UL register. In addition GPIOs peripheral can produce interrupts.

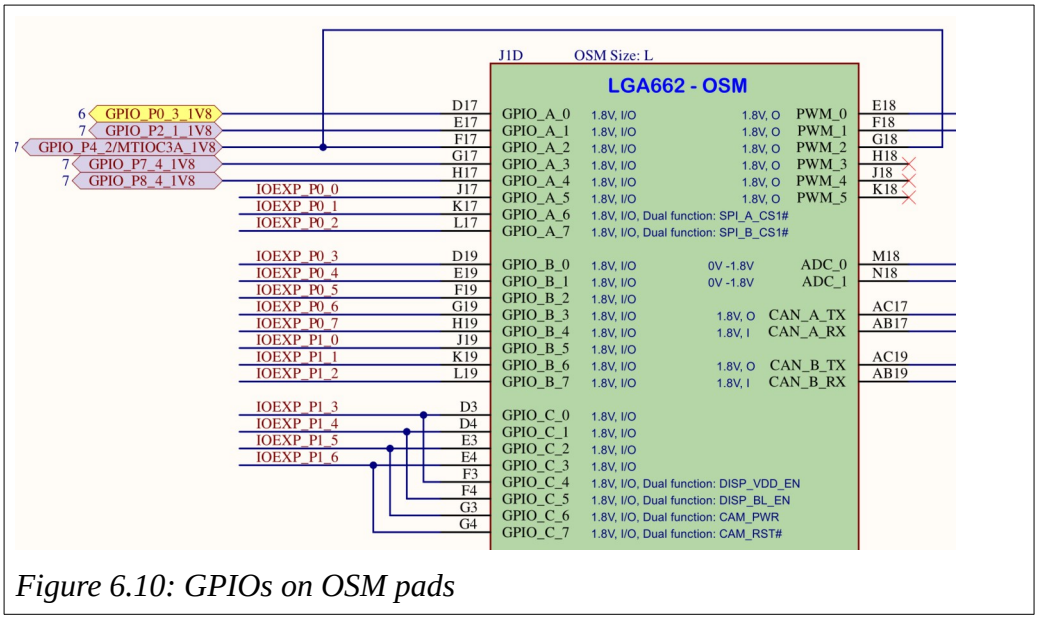


Figure 6.10: GPIOs on OSM pads

6.11 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1

v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the LGA contacts.

7. Power Supply

7.1 Power supply from base board

RNX-RZG2UL-OSM SoM is powered by regulated DC supply 5.0V

Signal	Type	Description
VSYS_5V	Power input	Main Power Supply 5.0V
GND	Power input	Common ground

7.2 System Signals

Signal	Type	Description
PWR_BTB#	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_RST#	Input	PMIC Reset signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	MIn	Max	Unit
VSYS_5V – Main Power Supply	-0.5	5.5	V

8.2 Recommended Operating Conditions

Parameter	MIn	Typ	Max	Unit
VSYS_5V – Main Power Supply	4.75	5.0	5.25	V
VSYS_5V – recommended source capability		3.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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